Class-DE Ultrasound Transducer Driver for HIFU Therapy

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***Abstract*—This paper presents a practical implementation of an integrated MRI-compatible CMOS amplifier capable of directly driving a piezoelectric ultrasound transducer suitable for high-intensity focused ultrasound (HIFU) therapy. The amplifier operates in Class DE mode without the need for an output matching network. The integrated amplifier has been implemented with the AMS AG H35 CMOS process. A class DE amplifier design methodology for driving unmatched piezoelectric loads is presented along with simulation and experimental results. The proposed design achieves approximately 90% efficiency with over 800 mW of output power at 1010 kHz. The total die area including pads is 2 mm^2. Compatibility with MRI was validated with B1 imaging of a phantom and the amplifier circuit.**

***Index Terms*—Biomedical electronics, Class DE amplifier, Ultrasonic transducer, HIFU, Magnetic resonance imaging**

I. Introduction

HIGH intensity focused ultrasound (HIFU), is a non-invasive surgical technique that thermally ablates tissue in human organs without the need of incision. Tissue ablation is achieved by focusing acoustic energy that translates into heat energy delivered to the focal zone of the ultrasound transducer [1] . HIFU operation can be guided by Magnetic Resonance Imaging (MRI) since this imaging modality provides high contrast volumetric information and it is capable of performing real-time monitoring of thermal effects [2], [3]. These developments often require the use of multi-element ultrasonic transducers. This allows controlling the location where the energy is focused by electronically driving each element at a different phase. The advantage of this approach is that different locations can be treated without physically moving the array. Using multiple independent elements increase the complexity of the connections and driving electronics required to pilot HIFU devices. There is considerable interest both at the research and commercial levels for developing new and improved electronic systems for HIFU that can drive multi-element devices with 1000 or more elements at an affordable cost. By providing a driving system that can pilot a large number of elements with enough power to achieve therapeutic levels, we could achieve the necessary degree of freedom to concentrate the HIFU energy where it is needed. Furthermore, this system should allow piloting devices that are under MRI guidance, providing thermal control for the therapy.

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This work reports progress towards that goal. We propose a MRI-compatible, integrated CMOS class DE amplifier that can directly drive a piezoelectric ultrasound transducer with high efficiency. The amplifier is intended to be mounted inside the transducer enclosure. High efficiency translates in low heat dissipation at the amplifier and thus simplified thermal management. The removal of the output matching network results in a more compact design and helps to overcome one of the challenges of developing an MRI-compatible device, *i.e.* to eliminate the use of magnetic components such as inductors. The work presented here expands previous work by the authors [4] in two ways: (1) a methodology to determine optimum excitation parameters for a given transducer is presented and (2) the amplifier has been fabricated and experimentally tested.

Most high power drivers for piezoelectric ultrasound transducers require external matching networks or external inductors that would interfere with the MRI-guidance system. In current designs these matching networks are located several meters away outside the MRI chamber or are near the transducer but require bulky air-core inductors. This increases the size and installation cost of the system. Hall and Cain [5] proposed a low-cost high-efficiency amplifier for driving transducer arrays; however, the proposed design requires an LC circuit with high-Q inductors. Compact high-Q inductors of suitable values require ferrite cores and are incompatible with the MRI environment. If these LC filters are omitted, the amplifier efficiency degrades and the square wave excitation causes the transducer to produce unwanted sidelobes in the acoustic power field [6]. These sidelobes will eventually distort the shape of the focal zone and the precision of the focusing point. Tang and Clement [6] evaluated the performance of the harmonic cancellation technique for a therapeutic ultrasound transducer in HIFU application. However, the proposed amplifier requires a transformer that cannot be integrated on-chip. Lewis and Olbricht [7] developed a high-efficiency amplifier for a high intensity ultrasound system application without using an external matching circuit, but exciting an ultrasound transducer with a square wave is not suitable for HIFU application and the design is not small enough for a compact solution. Ang et al. [8] have fabricated an integrated amplifier chip for ultrasound dental tissue healing. Although it has a power efficiency of 70% and an output power of 0.58W, it requires an external LC matching network. Recently, Bozkurt [9] proposed an 8-channel IC driver for an ultrasound catheter ablation system. The driver for each channel consists in a push-pull switch directly connected to a CMUT with an input capacitance of 20 pF at 10 MHz. That driver does not use

inductors and is likely to be compatible with MRI, but power efficiency and harmonic content are not discussed in that work. Several other integrated ultrasonic transducer drivers for sensing and imaging applications have been proposed in the literature, [10]–[14] are some examples. However these drivers are intended for producing sharp pulses instead of a continuous sine wave and are not suitable for HIFU.

The remainder of this paper is organized as follows: a piezoelectric transducer model for a class DE amplifier design is presented in Section II, followed by a proposed design methodology to determine the optimum parameters of the class DE amplifier and circuit design overview in Section III. Simulation and experimental results, including magnetic resonance imaging compatibility are presented and discussed in Section IV.

II. Transducer Model

The transducer used in this work is a piezo-composite crystal (DL47, DeL Piezo, West Palm Beach, FL) shaped as a section of sphere with a radius of 50 mm, a diameter of 25 mm and a thickness of 2.8 mm (Fig. 1). The transducer power efficiency is approximately 80 %. This transducer was measured using a vector network analyzer with a calibration procedure to remove the effect of cables and connectors. The crystal

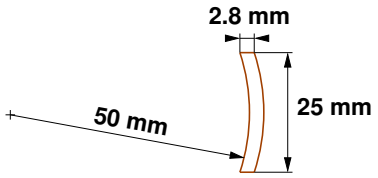

Fig. 1. Piezoelectric transducer geometry.

has a natural resonant frequency near 1 MHz. A piezoelectric resonator can be represented by the Butterworth Van Dyke (BVD) equivalent circuit and the detailed characterization for piezoelectric load for this work is discussed in References [4], [20]. For the purpose of amplifier tuning only the part of the

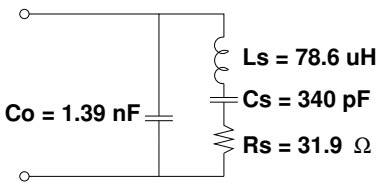

Fig. 2. Piezoelectric transducer simplified equivalent circuit.

equivalent circuit corresponding to the fundamental resonance is considered, as shown in Fig. 2. The reflection coefficient of the model is compared with the measured reflection coefficient in Fig. 3. The Q factor ($Q = \omega Ls/Rs$) of the equivalent circuit near 1 MHz is approximately 15. It is important to note that the driver has to be designed to work with that equivalent circuit with no external inductors. This rules out class E amplifiers. A regular class D amplifier would be inefficient because switches would have to turn on and off with a nonzero voltage applied to its terminals resulting in a waste of power. However it is

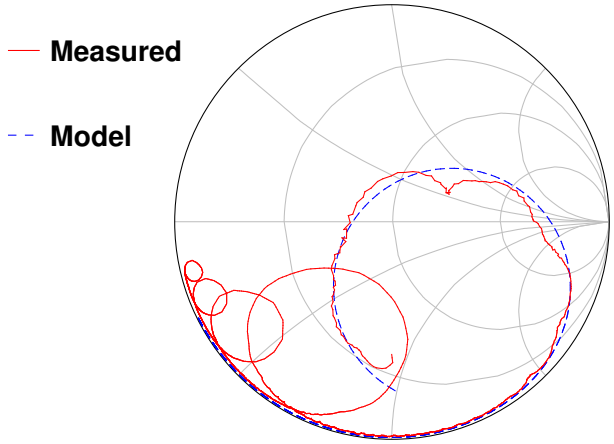

Fig. 3. Smith Chart with measured reflection coefficient and simplified model reflection coefficient.

possible to prevent this and achieve high efficiency by driving the amplifier in class DE mode.

III. Design Methodology

Fig. 4 shows a simplified schematic diagram of a class D amplifier operated in class DE mode. The parallel capacitor

$$C_p = C_0 + C_{SW} + C_{ext} \ ,$$

includes the transducer parallel capacitor (C_0), the parasitic capacitance of the switches (C_{SW}) and any additional external capacitance (C_{ext}). The duty cycle (D) is defined as follows:

$$D = \frac{t_{on}}{T} \ ,$$

where t_{on} is the conduction time and T is the period of the excitation. The switches are operated with a duty cycle between 0 and 0.5, usually close to 0.25. Fig. 5 shows the waveforms in class DE operation. The main feature of this

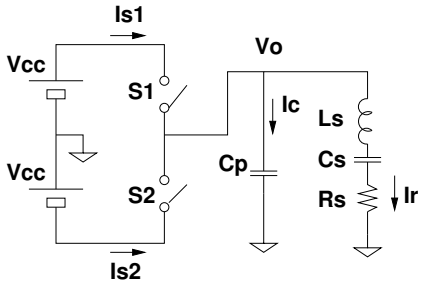

Fig. 4. Simplified schematic of a class DE amplifier.

operation mode is that losses in switches are minimized since at the time one switch closes, the voltage across the switch and its derivative are zero. This condition is often referred as zero voltage switching (ZVS) and zero derivative switching (ZDS). In order for this to happen, C_p must provide the load current while charging to a peak value equal to $\pm V_{cc}$ during the times that both S1 and S2 are open.

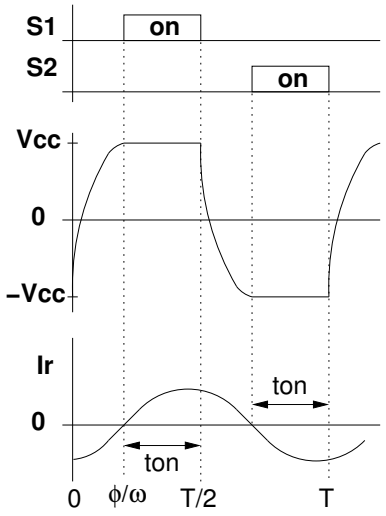

Fig. 5. Ideal waveforms in class DE amplifier.

A. Optimum frequency and duty cycle

Since the Q factor of the resonant branch is high, the resistor current (I_r) is almost sinusoidal and the following analysis is valid. The switches are assumed to have zero resistance. The reactance of the resonant branch at the frequency of operation (ω) is defined as:

$$X_S = \omega L_S - \frac{1}{\omega C_S} \ . \tag{1}$$

The condition for class DE operation (ZVS and ZDS) is that the impedance of the series branch ($R_S + jX_S$) satisfies the following equations [17]:

$$R_S = \frac{1-\cos(2\phi)}{2\pi\omega C_p} \tag{2}$$

$$X_S = \frac{2\phi-\sin(2\phi)}{2\pi\omega C_p} \tag{3}$$

where ϕ is an angle that depends on the duty cycle (see Fig 5):

$$\phi = \pi(1-2D) \ .$$

Equations (2) and (3) would normally be used to find the value of the external parallel capacitor and to design an impedance matching network for the load that provides the required impedance at the frequency of operation [17]. For the problem considered in this work, however, the load is fixed and the optimum frequency of operation and duty cycle must be determined. The following procedure is proposed here: solve for ω in Eq. (2):

$$\omega_r = \frac{1-\cos(2\phi)}{2\pi C_p R_S} \ , \tag{4}$$

substitute Eq. (1) in Eq. (3) and solve for ω:

$$\omega_x = \sqrt{\frac{2\phi-\sin(2\phi)}{2\pi C_P L_S} + \frac{1}{C_S L_S}} \ . \tag{5}$$

Class DE switching occurs when $\omega_r = \omega_x$ for a given value of D. By plotting the corresponding frequencies as a function of D, the optimum frequencies and duty cycles are found as shown in Fig. 6. In that figure, $f(R_S)$ and $f(X_S)$ are the frequencies corresponding to ω_r and ω_x, respectively. In this calculation C_{SW} was assumed to be 60 pF and C_{ext} was set to zero. From this graph we conclude that the transducer can

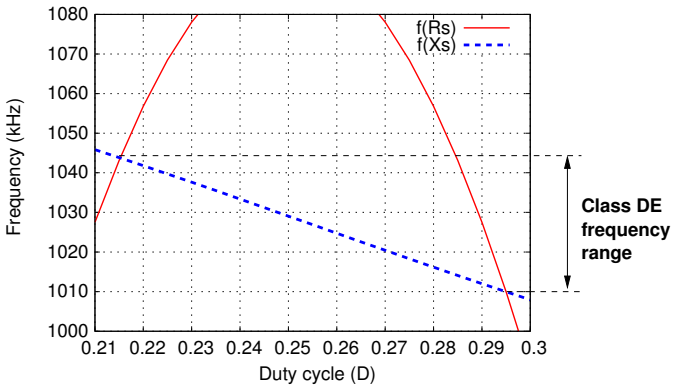

Fig. 6. Frequency range and duty cycle for class DE operation.

be driven in optimum class DE mode only at two frequencies: $f_1 = 1010$ kHz and $f_2 = 1045$ kHz with $D_1 = 0.295$ and $D_2 = 0.215$, respectively. If C_{ext} is increased, f_1 increases and f_2 decreases until they meet. The maximum C_{ext} that allows optimum operation with this transducer is 100 pF. In that case, there is a single optimum point at $f = 1024$ kHz with $D = 0.255$.

Since the transducer load is not exactly equal to the RLC circuit used for design, in practice the amplifier will operate slightly outside of the optimum condition. It has been shown [18] that the efficiency is not very sensitive to deviations in frequency and duty cycle. Sensitivity with respect to C_{ext} is also low [4]: when this transducer is driven at 1 MHz with C_{ext} up to 1 nF, the efficiency remains greater than 79 % with any value of D between 0.25 and 0.35 (these results were obtained using a different but conceptually similar chip design). This property is important because the transducer impedance has small variations due to changes in the surrounding acoustic environment and temperature. In the proposed application acoustic environment and temperature do not significantly change and thus a fixed tuning to typical conditions is acceptable.

For maximum load power given a constant supply voltage, the operating frequency must be closest to the series resonance frequency:

$$f_s = \frac{1}{2\pi\sqrt{L_S C_S}} = 973\text{kHz} \ .$$

Since in class DE mode the operating frequency must be greater than the series resonance frequency of the transducer (*i,e.*, $X_S(f_S) > 0$) [16] it follows that the operating frequency should be set to the lowest optimum value, $f_1 = 1010$ kHz.

B. Integrated driver design

The driver was implemented using the AMS AG H35 CMOS process. Fig. 7 shows a simplified schematic diagram of the proposed integrated amplifier. The output stage implements a Class DE amplifier. Only control logic, gate

drivers and switches are integrated: the output network has been replaced by a piezoelectric ultrasound transducer. The chip substrate is connected to the negative supply ($-V_{cc}$). A

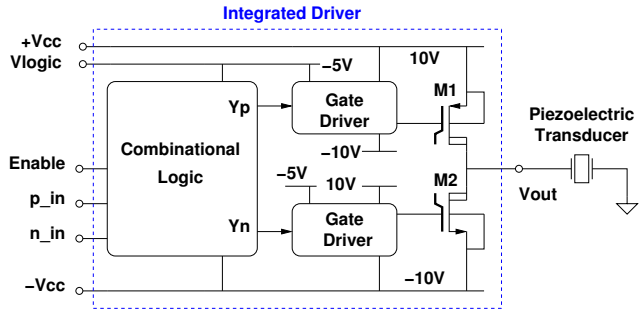

Fig. 7. Simplified diagram of proposed integrated driver.

micrograph of the chip is shown in Fig. 8. Several pads have been used for the high-voltage supplies and the output pin to reduce the current density. The switching transistors, M1

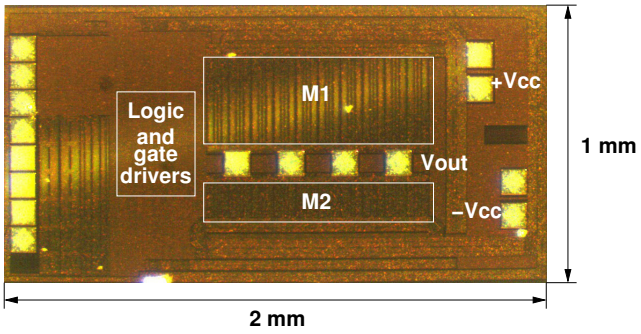

Fig. 8. Micrograph of the chip.

and M2 are implemented using high voltage MOS transistors. They are sized to provide the same on-resistance and this requires a wider PMOS transistor. This resistance should be as low as possible, but there is a trade-off between chip area, drain capacitance and on-resistance. For an on-resistance approximately equal to 2.3 Ω, M1 and M2 are designed according to Table I and they use most of the chip area. The combined drain capacitance is approximately 35 pF.

TABLE I
SWITCH TRANSISTOR PARAMETERS.

	M1	M2
Transistor finger W/L (μm/μm)	50/1.4	50/1
Number of parallel fingers	360	140

Two static level shifters [19] implement the gate drivers. They convert a 5 V logic signal to the ±10 V required for the amplifier stage. Another functionality of the gate drivers is to control the rise and fall time of the gate driving signals that feed the M1 and M2 switches. The drivers are designed to produce approximately the same rise and fall times in both switches. Schematic and design considerations for the level shifters are discussed in [4], [20]. The maximum supply voltage in this chip is currently limited to 20 V (±10 V) due to these shifters. With the same fabrication technology, this limit could be raised to 50 V using a different shifter design.

The combinational logic block provides the functions of power stage enabling, input buffering and protection from faulty input combinations. It is located prior to the gate drivers of the amplifier. It accepts a standard 5 V power supply, consisting of three inputs and two outputs. Table II summarizes the purpose of each input/output. The Enable pin is responsible

TABLE II
COMBINATIONAL LOGIC INPUTS AND OUTPUTS.

Pin	I or O	Description
Enable	I	Enables or disables the complete chip.
p_in	I	Logic input to drive M1
n_in	I	Logic input to drive M2
Yp	O	Signal for M1 gate driver
Yn	O	Signal for M2 gate driver

for the on-off function of the power stage. When the Enable input is low, both power transistors (M1 and M2) are biased in the cut off mode. When Enable is high, outputs will follow the respective inputs, except when a faulty input (p_in , n_in) = (0,1) is identified. This input would turn on both power transistors at the same time and cause a short circuit.

The same driver circuit could be used with different transducers as this chip is capable of operating in a wide frequency range up to several MHz with any $D < 0.5$. Tuning is performed by adjusting the operating frequency and duty cycle for optimum efficiency for a given transducer as outlined in Section III-A.

IV. RESULTS AND DISCUSSION

Fig. 9 shows the simulated output voltage of the designed chip driving the equivalent circuit of Fig. 2 as a load under the calculated optimum conditions with $f = 1010$ kHz and $D = 0.295$. The waveforms are close to ideal the ZVS and ZDS conditions are (practically) met. Fig. 10 shows the simulated

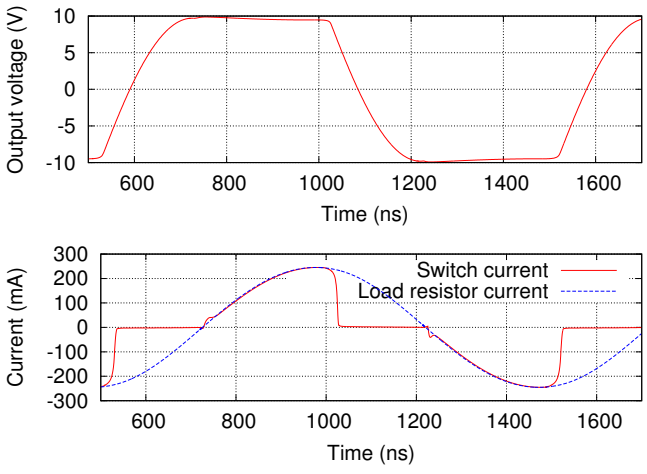

Fig. 9. Simulated output waveforms at 1010 kHz with $D = 0.295$ using the equivalent circuit of Fig. 2 as a load.

waveforms using an accurate transducer model. The transducer was modelled by fitting a high-order rational transfer function to the measured frequency domain reflection coefficient. It can be observed that the amplifier is now operating outside

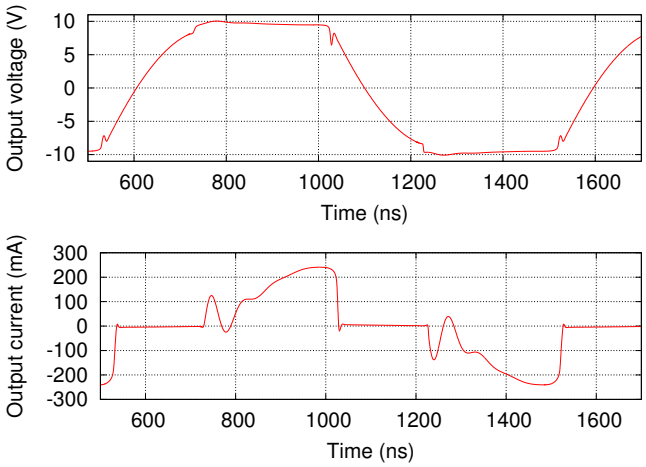

Fig. 10. Simulated waveforms at 1010 kHz with $D = 0.295$ using an accurate transducer model.

(but close) to the optimum condition. A duty cycle sweep was performed to analyze potential for improvement. The simulated efficiency and output power as functions of the duty cycle are summarized in Fig. 11. As expected [4], [18], an

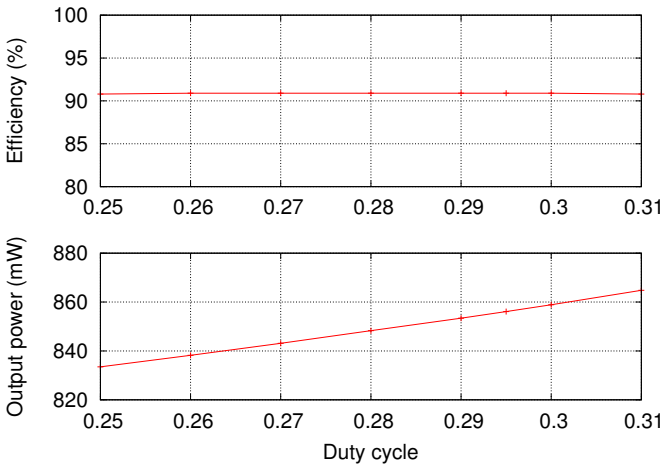

Fig. 11. Simulated efficiency and output power at 1010 kHz versus D.

increase in duty cycle results in a small increase in output power. The efficiency is almost constant.

The proposed integrated driver is intended to be attached at the back of a piezoelectric ultrasound transducer. For the reported measurements, as the transducer must be tested under water, a short section of coaxial cable was used to keep the driver outside of the water container and accessible for measurements as shown in Fig. 12. The output power was determined by averaging the product of the measured load voltage and current. A low resistance was connected in series with the transducer (R_1) to determine the load current. Figures 13 and 14 compare the simulated and experimental output current for $D = 0.290$. The simulated circuit was modified to account for the conditions of the experimental setup with the introduction of a series resistor (0.77 Ω), additional capacitances to account for the oscilloscope probes

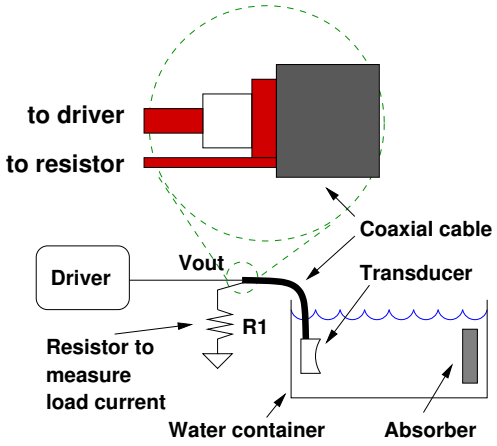

Fig. 12. Experimental setup diagram. $R_1 = 0.77\ \Omega$ is connected to the outer conductor (see inset) of the coaxial cable in series with the load and is used to determine the load current.

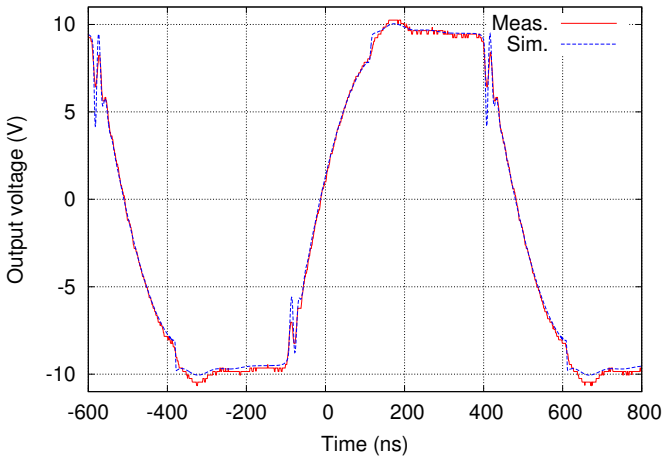

Fig. 13. Comparison of experimental and simulated output voltage at 1010 kHz with $D = 0.290$.

(20 pF in parallel with the driver and in parallel with R_1) and a transmission line to model the coaxial cable ($Z_0 = 50\ \Omega$, length= 190 mm, normalized propagation velocity= 0.674). The voltage waveforms agree almost perfectly but the experimental current waveform presents significantly more ringing than the simulated one. This discrepancy however has a small effect in the simulated prediction for efficiency and output power. As shown in Fig. 15, the simulated and experimental efficiency and output power versus duty cycle agree quite well. The output power level is somewhat lower compared to Fig. 11 due to the introduction of R_1. For the efficiency calculation only the power delivered by the ±10 V sources was considered. Both simulated and experimental results agree and the efficiency always remains high. These results suggest that a fine adjustment of the duty cycle of the gate-driving pulses may not be required for efficient operation.

The effect of the operation frequency is investigated in Fig. 16. The measured efficiency and output power with constant $D = 0.25$ are plotted as a function of frequency. As the measurements for this sweep were taken on a different day that for the duty cycle sweep, differences in water temperature

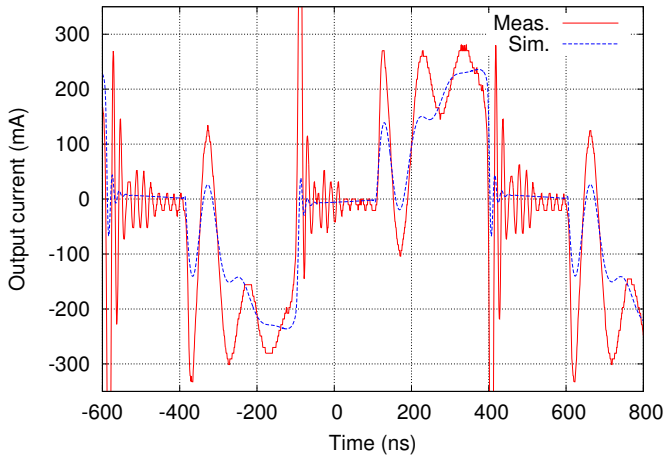

Fig. 14. Comparison of experimental and simulated output current at 1010 kHz with $D = 0.290$.

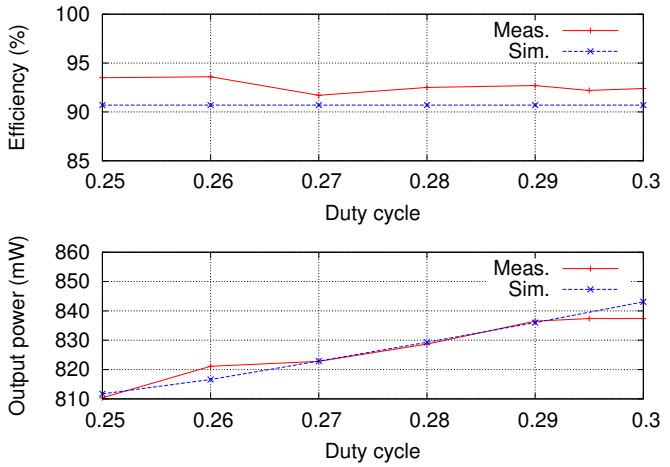

Fig. 15. Comparison between simulated and experimental results for efficiency and output power at 1010 kHz versus D.

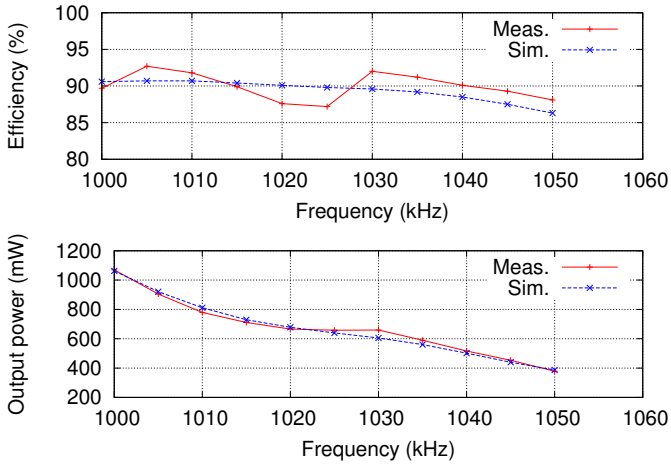

Fig. 16. Experimental and simulated results for efficiency and output power versus frequency with $D = 0.25$.

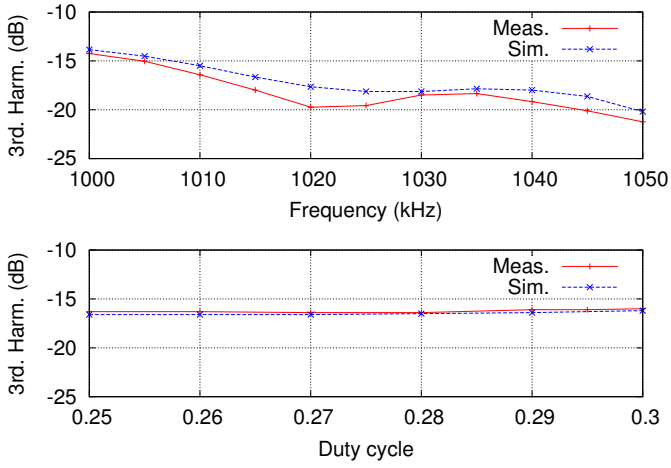

Fig. 17. Experimental and simulated results for the output voltage third harmonic level versus duty cycle with $f = 1010$ kHz and versus frequency with $D = 0.25$.

and transducer position in the water tank produce slightly different values for $f = 1010$ kHz. Nevertheless the values are close and the results agree with the expectations set by the theory. The output power decreases as the operating frequency is increased away from f_S. These results confirm the low sensitivity of efficiency with respect to frequency and duty cycle.

Experimental and simulated output voltage third harmonic level versus duty cycle and frequency is shown in Fig. 17. If the transducer is operated at 1010 kHz, the expected third harmonic level is -16.4 db. The third harmonic will be further attenuated approximately 9.6 dB [20] by the transducer for a total attenuation of 26 dB in the acoustic wave. Whether this third harmonic level will produce or not unacceptable sidelobes in the acoustic power field generated by a transducer array has not yet been determined. A small improvement in third harmonic reduction can be achieved by increasing the operating frequency at the expense of reduced output power (Fig. 16). Another alternative to reduce the third harmonic is to connect an external capacitor (C_{ext}) and operating at lower efficiency farther away from optimum conditions as shown in [4]. Another more promising alternative to be investigated is to excite some of the transducers in an array with the third harmonic in order to cancel any unwanted sidelobes.

A. *Magnetic resonance imaging compatibility*

As the driver is just a silicon die without any magnetic components, it is not expected to cause any artifacts in the MR image. To verify this, image quality was assessed in the presence of the chip. A standard small phantom was imaged using a SENSE Wrist coil 8 elements coil[1] in an 3T Achieva scanner. The chip was located immediately on top of the phantom and gradient echo images with and without the chip were subtracted (Gradient Echo, TE/TR$=$ 7.80/17, FOV$=$ 10 cm, Slice$=$ 5 mm, ETL$=$ 1, 1 NEX). A B1 map was also obtained with and without the chip to detect potential changes in homogeneity caused by the chip (Gradient Echo,

[1]Philips, The Netherlands

TE/TR= 7.80/531, FOV= 10 cm, Slice= 5 mm, ETL= 1, 1 NEX, dual flip angle).

The presence of the chip did not significantly alter the quality of the image as observed by an average SNR of 49.5 ± 2.3 dB without the chip and 47 ± 1 dB with the chip. An MR image of a phantom where the chip was located at the top is shown in Fig. 18. The image remains similar with (left) and without (right) chip and the subtracted and B1 map images show no visible impact of the chip.

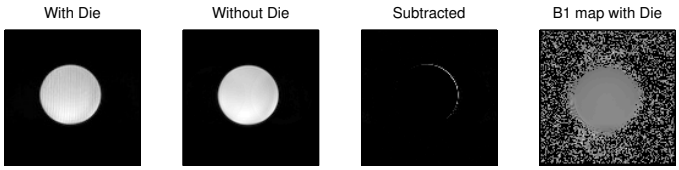

Fig. 18. Example MR images of the phantom with and without the chip and the corresponding subtracted and B1 map image with the chip.

B. Discussion

The proposed driver presents some shortcomings compared to alternative designs using external matching networks. These shortcomings and some possible workarounds are discussed in the next paragraphs.

Limited voltage supply range: this is not an intrinsic problem of class DE operation but just a limitation of this particular implementation. Even with this limitation the proposed driver would be adequate for transducer array with several hundreds of elements, as the power contribution of each individual transducer is small.

Operating frequency range: for efficient operation the frequency range is limited to a relatively small interval above the transducer's series resonance frequency. This range is enough to handle small changes in transducer impedance due to fabrication tolerances and/or relatively small changes in environmental conditions. If large environmental changes are expected, the frequency and duty cycle should be adapted for each condition.

Transducer compatibility: if C_0 in the transducer equivalent circuit is too high then it is not possible to achieve optimum class DE operation. Ideally transducers should be designed to admit at least one optimum operation point as described in Section III-A. The driver may still be usable even if no optimum operation point exists. In that case a numerical optimization procedure could be performed to tune frequency and duty cycle.

Output power control: output power can be controlled by varying the supply voltage, but this is a disadvantage compared to a standard class D amplifier with a load filter [21] that admits power control by varying the duty cycle.

Harmonic content: it is difficult to further reduce the third harmonic level present at the output. Some alternatives have been discussed earlier in this section but this is an area for improvement.

Several steps remain to be performed in order to produce a practical compact multi-element HIFU driver. Although it would be possible to drive a transducer array with this chip, the number of input signals with specific duty cycles would require too much external processing. More logic will be added in a future revision to simplify this. Also, a feedback circuit may be required to measure the power being sent to the transducer in real time to adapt the frequency/duty cycle according to changes in transducer impedance with the environment conditions.

V. CONCLUSION

This work has demonstrated the feasibility of directly driving a piezoelectric transducer for HIFU applications using a class DE amplifier. The elimination of the external matching network between the amplifier and the piezoelectric crystal results in a more compact design and MRI-compatibility. The proposed driver could be installed inside the transducer enclosure. High efficiency translates in low heat dissipation at the amplifier and thus simplified thermal management. The driver has a measured output power of 830 mW at 1010 kHz with an efficiency over 90 %. The output voltage third harmonic level is -16.4 dB below the fundamental. The total chip area, including pads is 2 mm^2.

The driver has been tested with one particular transducer, but it can also be used with other transducers as long as the conditions presented in Section III-A are satisfied. Only the amplifier excitation needs to be modified. Another conclusion from the results presented here is that a very fine control of the duty cycle is not critical for efficiency nor harmonic performance. Efficiency is always high if duty cycle tolerance is within ± 0.025 for the tested case. On the other hand as the duty cycle can not be varied in a wide range, output power control of an individual amplifier would require a variable supply voltage.

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