An Integrated Full-Bridge Class-DE Ultrasound Transducer Driver for HIFU Applications

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***Abstract*—This paper presents an integrated MRI-compatible full-bridge Class-DE ultrasound transducer driver design for HIFU applications. This design includes a digital logic unit to individually control the phase and duty ratio of each transducer when the driver is used in an array configuration. This work also shows the performance of the proposed driver with three different ultrasonic transducers. Simulation results predict at least 89% efficiency for the two transducers that support ideal Class-DE operation without matching networks. The proposed driver has been implemented by using AMS AG H35 CMOS process. The total die area of the driver is 3 mm^2.**

I. Introduction

High intensity focused ultrasound (HIFU) is a non-invasive surgical technique that ablates human tissues by focusing ultrasound on the point of interest. The focus location of the ultrasound wave can be controlled using phased array transducers, and magnetic resonance imaging (MRI) is used for guidance since this imaging technique provides high contrast volumetric information and it is capable of performing real-time monitoring of thermal effects [1], [2].

The objective of our work is to design a compact ultrasound transducer driver to be used in an array configuration and the driver has to be compatible with the MRI environment. To reduce the connection complexity in an array configuration, the number of electrical inputs of each driver must be minimized and, if possible, these inputs should be shared among different drivers. Thus the proposed driver includes a digital logic unit that makes the driving pulse trains phase shift and duty ratio programmable. To increase MRI compatibility, the driver aims to operate some types of piezoelectric transducers efficiently without the need for matching networks. Matching networks usually require inductors that could interfere with the image quality in MR.

There are some published works that relate to our goal. Hall and Cain [3] proposed a highly-efficient Class-D amplifier to drive the transducer, but they used a LC network for matching circuit which cannot be used in MRI. Tang and Clement [4] used the harmonic cancellation technique for the HIFU application, but the amplifier that they proposed require a transformer which is also not MR compatible. Our research group previously presented an integrated driver [5], [6] that operates in class DE mode and does not require magnetic components. The driver presented in this paper is an improvement over that original design.

II. Transducer Characterization

A. Physical Parameters and Equivalent Circuit

The impedance of all transducers was measured using a vector network analyzer with a calibration procedure to remove the effect of the cables and connectors. The dimensions, series resonance frequency (f_S) and parallel resonance frequency (f_P) for the transducers used in this work are listed on Table I. All transducers are made of a piezo-composite crystal (DL47, De Piezo, West Palm Beach, FL) and have circular shape. Transducer A is shaped as a flat disc and comes from an array used for cell sonoporization [7]. Transducer B is a curved disc shaped as a section of sphere with a radius of 50 mm [6]. Transducer C is ring-shaped [8] and has two input ports. In this work only the 'propagation' (connected to the top and bottom plates on the ring) port is exited by the proposed driver.

TABLE I: Transducer parameters

Transducer	A	B	C
Diameter (mm)	20	25	12
Internal Diameter (mm)	n/a	n/a	3
f_S (kHz)	1000	973	510
f_P (kHz)	1110	1086	518

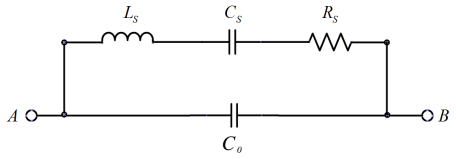


Fig. 1: Transducer equivalent circuit model

The piezoelectric resonator in the transducer can be represented by a Butterworth Van Dyke (BVD) equivalent circuit (Fig. 1) and every component of this equivalent circuit is calculated from the measured f_S, f_P and the impedance of resonator at its series resonance (Z_S) using the following equations [5]:

$$C_0 = \frac{-Im(Z_S)}{2\pi f_S |Z_S|^2} \quad (1)$$

$$R_S = \frac{|Z_S|^2}{Re(Z_S)} \quad (2)$$

$$C_S = C_0 \left[\left(\frac{f_P}{f_S} \right)^2 - 1 \right] \quad (3)$$

$$L_S = \frac{1}{(2\pi f_S)^2 C_S} \quad (4)$$

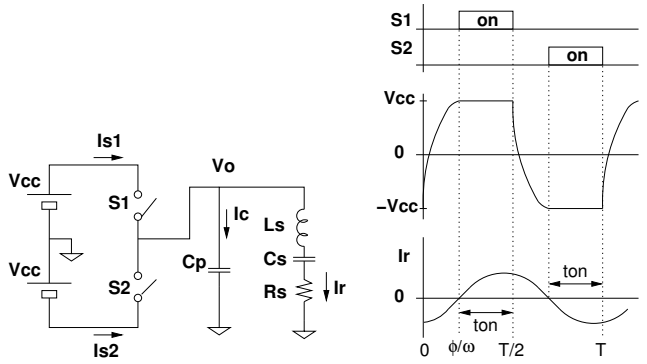
This equivalent circuit has the same topology of the required load for a class DE amplifier [9] and it is used to determine the optimum excitation parameters for the amplifier switches. The extracted circuit components are summarized in Table II

TABLE II: Circuit component values for all transducers

Transducer	C_0 (pF)	C_S (pF)	L_S (uH)	R_S (Ω)
A	664	154	164.3	42.1
B	1390	340	78.6	31.9
C	473	15	6500	1116

B. Optimum Operating Frequency and Duty Ratio

Figure 2a shows the schematic of half-bridge class DE amplifier. Figure 2b shows the ideal waveforms in class DE operation [9]. The key feature to achieve high efficiency is that the switch voltage is zero with zero derivative when the switch is turned on. We will consider that the switches in the



(a) (b)

Fig. 2: (a) Ideal Class-DE amplifier; (b) Ideal waveforms in class DE amplifier. From top to bottom: pulses in switches, load voltage and current in the series branch of the load

amplifier are loaded with the equivalent circuit of Fig. 1 plus an additional parallel capacitance,

$$C_p = C_0 + C_{SW} + C_{ext} \ ,$$

where C_{SW} is the parasitic capacitance of the switches and C_{ext} is an additional external capacitance (if present). The real and imaginary parts of the series branch of the load (R_S, X_S) must satisfy [9]:

$$R_S = \frac{1 - \cos(2\phi)}{2\pi\omega C_p} \quad (5)$$

$$X_S = \frac{2\phi - \sin(2\phi)}{2\pi\omega C_p} \quad (6)$$

where ϕ is an angle that depends on the duty cycle (see Fig 2b):

$$\phi = \pi(1 - 2D) \ .$$

In (5) and (6), the load is assumed to be fixed, so we solve the equations for ω and D [6] and if a solution exists, these values are the optimum operating frequency and corresponding duty ratio for class DE operation. For example, for transducer A, we obtain 2 solutions: ($f_1 = 1022$ kHz, $D_1 = 0.365$) and ($f_2 = 1087$ kHz, $D_2 = 0.175$). The operating frequency must be closest to the transducer's series resonant frequency to deliver a maximum power to the load. That means we should use f_1 and D_1.

Some transducers cannot be driven using this strategy. For instance, there is no solution of (5) and (6) for transducer C. In this case, either an external matching network (with inductors) is required or the amplifier has to be driven in sub-optimal conditions near the series resonance frequency of the transducer. This is further discussed in Section IV. The optimum Class-DE frequencies and duty ratios for transducers A and B are listed in Table III.

TABLE III: Optimum Class-DE driving parameters

Transducer	Duty Ratio	Optimum Frequency (kHz)
A	0.365	1013
B	0.295	1010

III. Proposed Design

The proposed transducer driver has a Class-DE full-bridge amplifier as the output stage and a logic control part which makes the duty ratios and operating frequencies programmable. Fig. 3 shows the structure of this driver and Fig. 4 shows the annotated layout. The driver has been implemented using the AMS AG H35 CMOS process. The total area including pads is 2×1.5 mm^2.

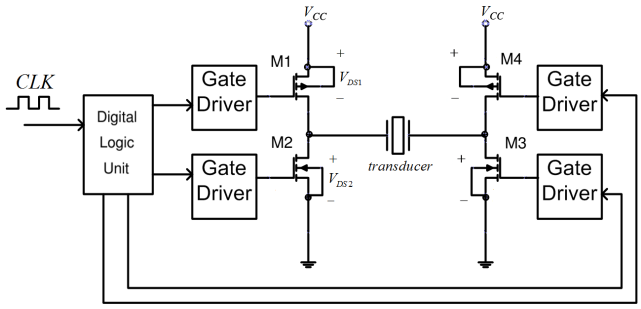


Fig. 3: Block diagram of the transducer driver

A. Output Stage

The output stage of the proposed driver can be seen as the combination of two half-bridge Class-DE amplifiers, their outputs are connected to the transducer terminals. Compared to the previously designed push-pull Class-DE amplifier [6], the full-bridge Class-DE amplifier can deliver 4 times the output power with the same DC supply voltage. Another advantage is that the number of external connections is reduced by

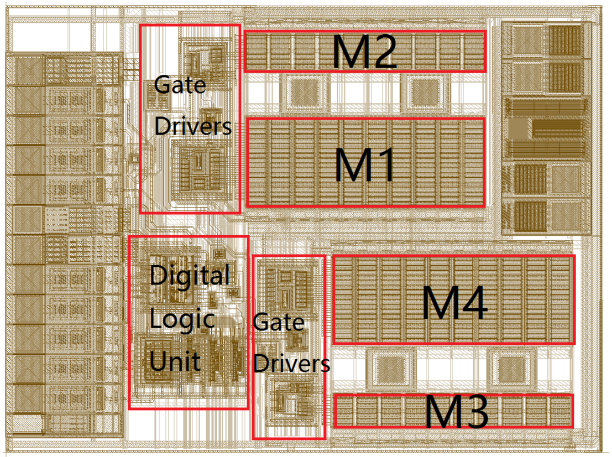


Fig. 4: Annotated layout

one as there is no need for a splitted DC power supply. These advantages come at the expense of double chip area to accommodate four transistors instead of two.

The driving strategy of the full-bridge Class-DE amplifier is similar to the half-bridge amplifier. Transistors M1 and M3 in Fig. 3 operate in the same way as S1 in Fig. 2a, while transistors M2 and M4 operate in the same way as S2. By using this method, there is no need for a splitted power supply.

B. Digital Logic Unit

A digital control unit is integrated on the proposed driver to program the phase and duty ratio of the Class-DE amplifier. The structure of this digital unit is shown in Fig. 5. There are 7

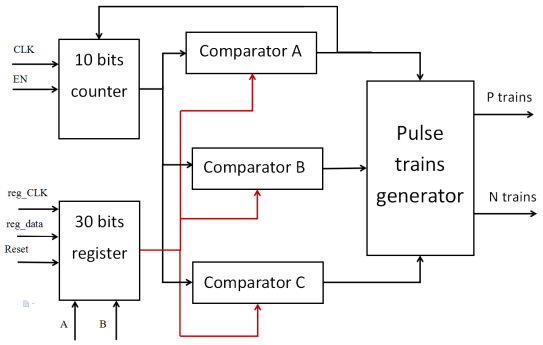


Fig. 5: Structure of digital logic unit

logic input pins. Among these, **CLK**, **EN**, **reg_CLK**, **reg_data** and **reset** are common to all drivers in an array. Pins **A** and **B** are used to address individual drivers in the array. As the power supply pins are also common to all drivers, this arrangement simplifies the the connection complexity in a transducer array.

When the **EN** input goes high, the 10-bit Counter counts the number of external clock signal's pulses (**CLK**). The external **CLK** is normally set to a multiple of the transducer operating frequency. The counter's modulus controls the resolution of the duty ratio and phase shift. The modulus of the counter must be set to half the period. Thus M_1, M_3 will be turned on in the first round and M_4, M_2 will be turned on in the second round. For example, if the counter's modulus has been set to 100, the duty ratio resolution is 0.5%, if we set the modulus to 50, the resolution will be 1%.

The 30-bit register has been divided into 3 parts, each part has 10 bits. The first part is the number of **CLK** pulses to be counted for one period of the output waveform, the second and third part are counts for turning one switch on and off, respectively, in each semi-period. These values define the duty ratio and the relative phase of the driver. For example, suppose that an external clock frequency of 202.6 MHz is used with Transducer A (*i.e.*, 200 times the load frequency), then the three values to program a duty ratio of 0.365 and a phase shift of 18° are: 100, 10, 83. The following is a summary of the digital logic operation when the chip is used in an array configuration:

1) Select the driver by setting both **A** and **B** to high and program the phase and duty cycle by loading the 30-bit register.
2) When all drivers in the array are programmed, set the **EN** pin to logic high to let counter start counting.
3) The pulse trains generator will generate the intended pulse trains to turn on and off the transistors in the Class-DE amplifier.

A simulation of the digital logic unit is shown in Fig. 6. Pulse trains are programmed for an output frequency of 20 MHz, 36° phase shift and 20% duty ratio. The corresponding register values are: 5, 1 and 3 with a clock frequency of 200 MHz. As the resolution in this example is very low, the error in phase shift is significant, but that error can be made negligible by selecting a higher resolution.

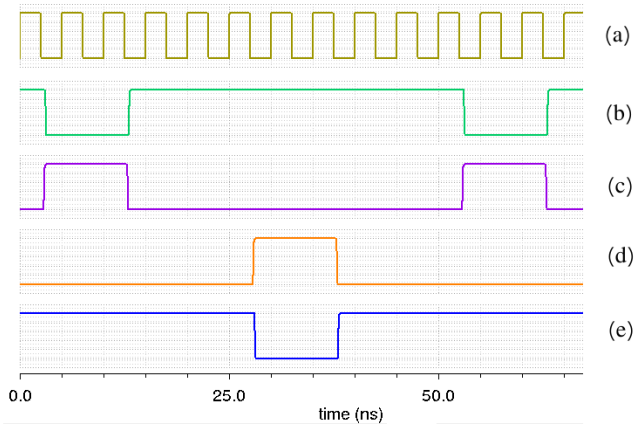


Fig. 6: Simulation results of digital logic unit; (a) External CLK signal; (b) Driving signal for M1; (c) Driving signal for M3; (d) Driving signal for M2; (d) Driving signal for M4.

IV. Simulation Results

All simulations presented in this paper were performed using the Spectre simulator (Cadence Design Systems, USA). For improved accuracy, transducers in simulations are modelled with a high-order rational function fitted to the measured scattering parameters (Spectre's "nport" model). Figures 7 and

8 show waveforms for Transducer A and B, respectively using the driving parameters from Table III. The output waveforms are clearly in class-DE mode. Only low amplitude switching peaks can be observed.

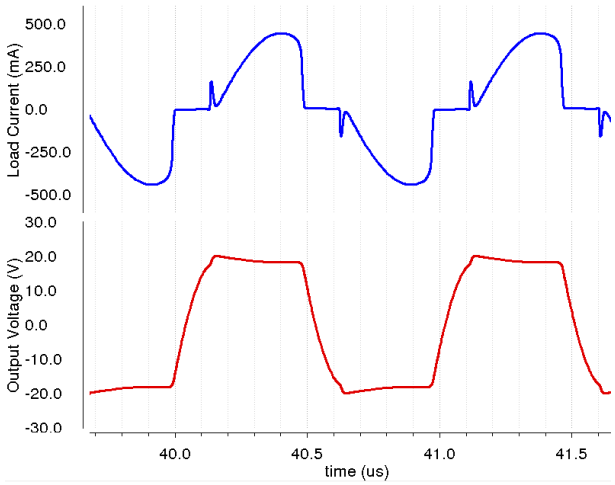


Fig. 7: Output waveforms for Transducer A

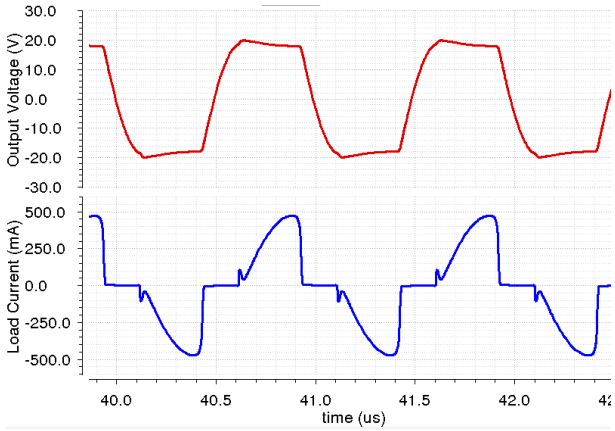


Fig. 8: Output waveforms for transducer B

As discussed in Section II, Transducer C can not be driven in ideal class DE mode. It was determined by simulations that when the transducer is driven at the series resonant frequency the efficiency has a peak for a duty ratio of 25%. The corresponding output waveforms for that condition are shown in Fig. 9. The amplifier is not operating in Class-DE mode and the output current waveform has high peaks, caused by the transistors turning on when the voltage across the drain and source is not zero. The average current peak value is 1.06 A. Table IV summarizes DC supply power, output power and efficiency for the three transducers.

V. Conclusion

The design of an integrated full-bridge Class-DE ultrasound transducer driver suitable for an array configuration has been presented. It was shown that the same driver is capable efficiently driving different transducers without the need for matching networks by just changing the driver's clock frequency and reprogramming the duty cycle. However, some transducers can not be efficiently driven in this way. The next planned step is to experimentally test the proposed amplifier.

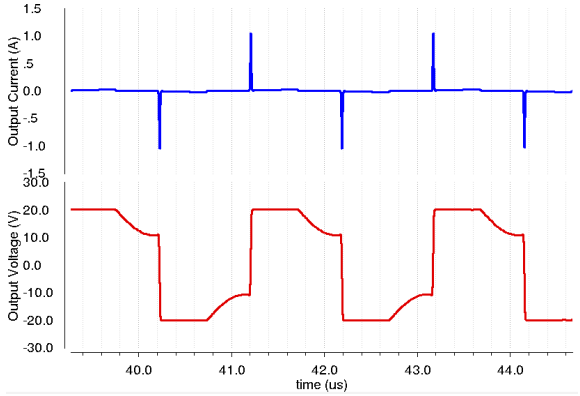


Fig. 9: Output waveforms for transducer C

TABLE IV: Power and efficiency summary

Transducer	DC Supply Power(W)	Output Power(W)	Efficiency(%)
A	4.38	3.93	89.9
B	4.02	3.59	89.4
C	0.524	0.227	43.3

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