Sub-1 V, 4 nA CMOS Voltage References with Digitally-Trimmable Temperature Coefficient

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***Abstract*—Two architectures for MOS-only low power voltage references with digitally-trimmable temperature coefficient are proposed in this work. A test chip implements them in a 0.35 μm CMOS process. A design methodology for both architectures, performance figures and preliminary test results are presented. Each circuit consumes around 4 nA and operates down to 0.95 V or better with a simulated temperature coefficient of 18 ppm/°C in the -20 °C to 80 °C range.**

I. Introduction

A voltage reference is one of the fundamental building blocks used in various devices such as A/D and D/A converters, sensor interfaces, and instrumentation circuits. The performance of the aforementioned devices strongly depends on how constant the voltage reference maintains its output voltage with changes in supply voltage and temperature. In addition, most voltage reference designs are susceptible to random process variations that may result in a performance worse than originally designed for. Moreover, many designs use resistors, which may vary in value by $\pm 20\%$ or more due to random process variations [1], and take up a very large chip area, in particular for circuits operating in the order of nW or less. Traditional designs also may use too much power for some applications such as medical implantable devices and energy-scavenging circuits. To overcome these limitations, voltage reference circuits using only MOSFETs have been proposed in the past [2]–[6]. Previous work had shown that it is possible to design a MOSFET-only voltage reference based on properties of constant inversion level biasing [7]. This work proposes, and implements for the first time, a practical reference of this kind by including a means to digitally trim its temperature coefficient.

Two alternative designs are proposed. Each design uses external digital signals to trim one of the following: (i) the aspect ratio of a diode-connected MOSFET load (Fig. 2b) or (ii) the load biasing current (Fig. 2a). These adjustments allow the circuit to be fine-tuned to present minimal voltage variations over a large temperature range, regardless of the random process variations that affect the temperature dependence of transistor parameters.

II. ACM Model

This section follows [7], [8] in describing the Advanced Compact MOSFET (ACM) model [9], [10] which is a continuously differentiable model that is consistent through all operating regions of the MOS transistor. The drain current through a MOS transistor is characterized by the difference of forward and reverse currents:

$$I_D = S\, I_{SQ}\ (i_F - i_R)\,, \tag{1}$$

where i_F and i_R are the forward and reverse inversion coefficients, respectively, S is the transistor width/length ratio (W/L), and I_D is the drain current. I_{SQ} is the technology-dependent sheet normalization current defined as:

$$I_{SQ} = \frac{1}{2}\, n\, \mu\, C_{ox}\, {U_T}^2\ ,$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance, n is the sub-threshold slope factor, and $U_T = kT/q$ is the thermal voltage, where k is Boltzmann's constant, q is the electron charge and T is the absolute temperature.

Inversion levels are related to transistor terminal voltages by the following close approximate equation:

$$\left(\frac{V_G - V_T}{n} - V_{S(D)}\right) \cong U_T\ \mathcal{F}(i_{F(R)})\ , \tag{2}$$

where V_G , V_S and V_D are respectively the gate, source, and drain voltages referred to bulk, V_T is the threshold voltage and

$$\mathcal{F}(i_{F(R)}) = \sqrt{1 + i_{F(R)}} - 2 + \ln\left(\sqrt{1 + i_{F(R)}} - 1\right)\ . \tag{3}$$

If i_F is much larger than i_R , the transistor is considered to be operating in saturation and i_R can be neglected. In saturation, i_F determines the inversion level of the transistor, where $i_F \in$ (0,1), [1,100), [100,∞) represents weak, moderate and strong inversion respectively.

III. Voltage Reference Concept

The basic topology for the voltage reference circuit [7] along with the current source it requires is described in this section. Fig. 1 shows a constant inversion level (i_F is constant)

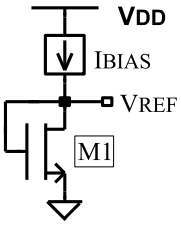


Fig. 1: Basic voltage reference circuit

current that biases MOSFET M1. Being diode-connected, M1 operates in saturation and Eq. (1) can be approximated as:

$$I_{D1} = S_1 \, I_{SQ} \, i_F \ . \tag{4}$$

As $V_G = V_{REF}$ and $V_S = 0$, from Eq. (2),

$$\mathcal{F}(i_F) = \frac{V_{REF} - V_T}{n \, U_T}. \tag{5}$$

The thermal voltage (U_T) can be written as:

$$U_T = U_{TR} \, \frac{T}{T_R} \ , \tag{6}$$

where U_{TR} is the thermal voltage at an arbitrary reference temperature T_R (usually 300 K). The threshold voltage dependence with temperature is well approximated as [11]

$$V_T = V_{T0} + K_{VT} \frac{T}{T_R} \ , \tag{7}$$

where V_{T0} is the extrapolation of the threshold voltage at 0 K and K_{VT} (usually negative) is defined as:

$$K_{VT} = T_R \, \frac{\partial V_T}{\partial T} \ .$$

By substituting Eq. (6) and (7) into Eq. (5), the expression becomes:

$$V_{REF} = V_{T0} + \frac{T}{T_R} \left(n U_{TR} \mathcal{F}(i_F) + K_{VT} \right) \ . \tag{8}$$

The condition for a temperature-independent V_{REF} is obtained when the second term in Eq. (8) is set to zero (thus $V_{REF} = V_{T0}$):

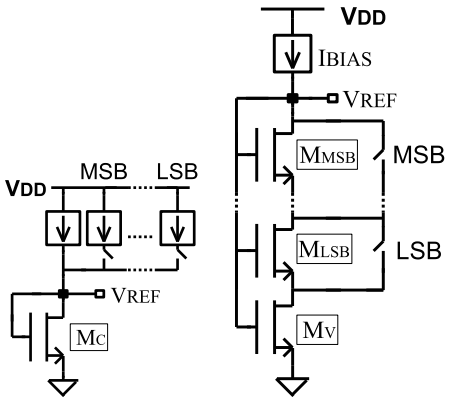
$$\mathcal{F}(i_F) = \frac{-K_{VT}}{n \, U_{TR}} \ . \tag{9}$$

Due to process variations, K_{VT} can not be accurately predicted and hence i_F must be 'trimmed' to compensate for variations. From Eq. (4) there are two possible ways to trim i_F: (i) adjust I_{D1} or (ii) adjust S_1, as illustrated in Fig. 2. Both of these architectures are explored in this work.

The constant-inversion level current source required to bias the voltage references of Fig. 2 is shown in Fig. 3 and is a variation of the current source used in [7]. Both the PMOS and NMOS current mirrors are cascoded for higher PSRR. N3 and N4 form a self-cascoded transistor that results in area savings [12]. The output bias current is [7]:

$$I_{BIAS} = a \left(S_{N2} \, i_{F_{N2}} \, I_{SQ} \right) \ ,$$

where a is the gain of the output branch of the PMOS current mirror. This gain is trimmable in the architecture of Fig. 2a.



(a) Constant load (b) Variable load

Fig. 2: Proposed voltage reference architectures

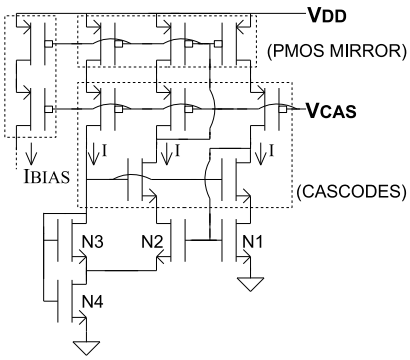


Fig. 3: Constant inversion level current source

Transistor ratios along with the PMOS mirror gain determine the inversion level (i_F). For good matching, the same NMOS unit transistor is used in the current source and the diode-connected loads.

IV. Design Considerations

This section outlines how the required range and resolution of i_F are obtained as well as how to implement the load and current source for each architecture.

A. Range of i_F

The temperature coefficient (TC) of the voltage reference is defined as follows:

$$TC = \frac{\partial V_{REF}}{\partial T} \, \frac{1}{V_{REF}} = \alpha_T \, \frac{1}{V_{REF}} \ , \tag{10}$$

where V_{REF} is the average output voltage throughout its temperature range. From Eq. (8),

$$\alpha_T = \frac{1}{T_R} \left(n U_{TR} \mathcal{F}(i_F) + K_{VT} \right) \ . \tag{11}$$

Neglecting the temperature dependence of n, the required range of i_F is determined by the dispersion of K_{VT} due to process variations. By setting $\alpha_T = 0$ in Eq. (11), $i_F = \mathcal{F}^{-1}(-K_{VT}/nU_{TR})$ is calculated for each extreme

of the K_{VT} range. Since data on this dispersion was not available among the technology parameters, information based on measurements from an existing device fabricated with the same technology plus an extra safety margin was used to determine the range of i_F.

B. Resolution of i_F

As i_F is trimmed in discrete steps (Δi_F), α_T cannot be made to exactly equal zero. Near $\alpha_T = 0$, from Eq. (11), a step in α_T is bounded by

$$\Delta\alpha_T \leq \frac{n\,U_{TR}\;\frac{d\mathcal{F}(i_F)}{di_F}\Big|_{MAX}}{T_R}\;\Delta i_F\;. \tag{12}$$

In Eq. (12) the maximum of $d\mathcal{F}(i_F)/di_F$ occurs at $i_{F_{MIN}}$. Taking the equality sign in Eq. (12) and a tolerance window of $\pm\alpha_T$, the maximum acceptable Δi_F is obtained:

$$\Delta i_F = \frac{2\,T_R\,\alpha_T\,\left(\sqrt{1+i_{F_{MIN}}}-1\right)}{n\,U_{TR}}\;. \tag{13}$$

This guarantees that a Δi_F step results in a $2\alpha_T$ step or lower.

C. Number of Bits

The switches depicted in Fig. 2 are implemented with transistors. These trimming transistors are arranged in a bit-wise manner, with the least-significant-bit (LSB) producing the smallest change of i_F (Δi_F) and each successive bit increasing the change by powers of two. With the range and resolution of i_F established, the number of bits required can now be determined as follows:

$$\frac{i_{F_{MAX}} - i_{F_{MIN}}}{\Delta i_F} \leq 2^N - 1\;, \tag{14}$$

where N is the number of bits as well as the number of trimming transistors required.

D. Biasing Strategy

Minimum consumption is limited by the errors introduced by leakage currents (I_{LEAK}) in reverse-biased drain/source junctions and off-state currents (I_{OFF}) through the switch transistors. To maintain the desired TC, Eq. (15) must be fulfilled

$$\frac{\sum I_{LEAK} + \sum I_{OFF}}{I_{MIN}} \leq \frac{\Delta i_F}{i_{F_{MIN}}}\;. \tag{15}$$

$\sum I_{LEAK}$, in turn, depends on the number of unit transistors in MV (Fig. 2b):

$$N_T = \frac{i_{F_{MAX}}}{\Delta i_F}\;. \tag{16}$$

In this work, MC in Fig. 2a uses the same unit transistors as MV in Fig. 2b.

V. Design Summary

A test circuit was designed and fabricated on a 0.35 μm CMOS technology to check both architectures. Table I outlines the design values and choices made based on Section IV and Table II shows the NMOS transistor dimensions used. S_U is the width/length ratio of the unit transistor. S and P indicate that the unit transistors are connected in series or parallel, respectively.

TABLE I: Design values and choices

i_F Range	37–59
$TC = \alpha_T/V_{REF}$	5 ppm/°C
N	6 bits
$I_{D,N2}$ (Fig. 3)	0.6 nA
$I_{D,MC}$ (Fig. 2a)	1–1.6 nA
$I_{D,MV}$ (Fig. 2b)	1.2 nA

TABLE II: NMOS transistor sizes

S_U	1 μm / 24.9 μm
(Fig. 3) N1, N2, N3, N4	2(P), 16(P), 20(S), 22(S)
(Fig. 2a) MC	130(S)
(Fig. 2b) MV, [MSB, …,LSB]	106(S), [32(S), 16(S), 8(S), 4(S), 2(S), 1]

VI. Results and Discussion

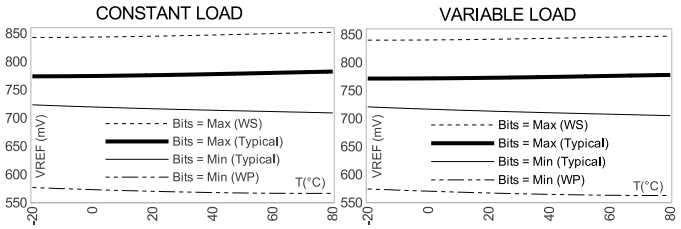


Fig. 4: Simulated V_{REF} as a function of temperature

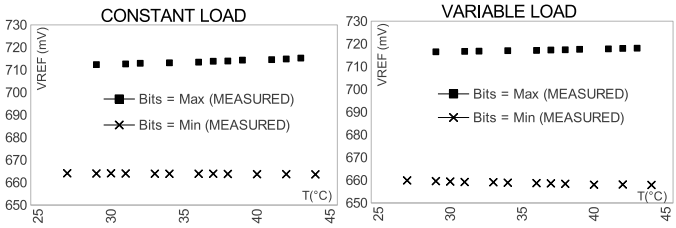


Fig. 5: Preliminary measurements for V_{REF} as a function of temperature

Fig. 4 and Fig. 5 show simulation results and preliminary measurements for V_{REF} as a function of temperature, respectively. The effect of setting the trimming bits for maximum positive or negative TC for typical parameters is shown in Fig. 4. Simulations for worst-case scenarios are also included.

The preliminary measurements as per Fig. 5 exhibit a similar behaviour of V_{REF} with respect to temperature, and are well within the worst-case tolerances. These results imply that there exists an optimum trimming in which the voltage reference will exhibit an output with the minimum TC.

Although the circuit was designed for a TC of 5 ppm/°C as per Table I, simulation results (Fig. 6) show about 18 ppm/°C for both architectures. This discrepancy is possibly due to second-order effects not considered in the design methodology. The experimental TC value for a wide temperature range still has to be measured.

The variation of V_{REF} as a function of the supply voltage at a temperature of 20 °C for both architectures is presented in Fig. 7. Dashed lines depict the worst-case process variations

TABLE III: Comparison of post-layout simulation results with other designs

	Constant Load	Variable Load	[2]	[3]	[4]	[5]	[6]
CMOS Technology (μm)	0.35	0.35	0.5	0.35	0.35	0.18	0.13
Voltage (V)	0.95–3.3	0.95–3.3	3.7	0.9–4	1.4–3	0.45–2	0.5–3
Current (nA)	4.3	3.3	378000	40	214	5.8	0.0044
TC (ppm/°C)	17.96	17.54	145	10	15	165	<50 (post trim)
V_{REF} (mV)	755	755	1121.9	670	745	257.5	176
PSRR (dB)	-44.1	-44.4	-45	-47/-40	-45	-40/-12	-53/-62
Area (mm^2)	0.048	0.053	0.4	0.045	0.055	0.043	0.00135

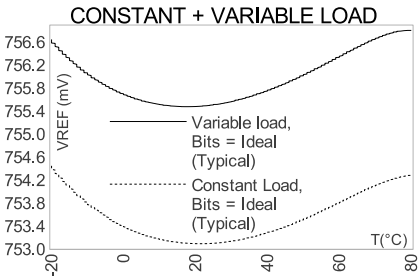


Fig. 6: Simulated V_{REF} as a function of temperature after trimming

that can occur as predicted by post-layout simulations, which are denoted by WS (Worst Speed) and WP (Worst Power). Points depict measured values when the trimming bits have been set for both $i_{F_{MIN}}$ and $i_{F_{MAX}}$.

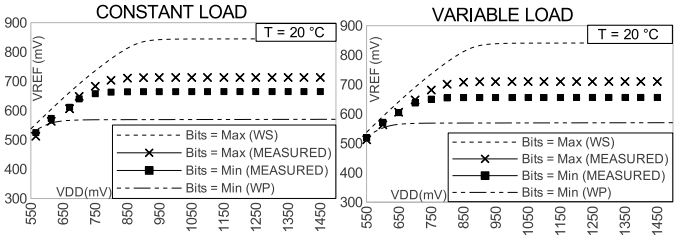


Fig. 7: Simulated and measured V_{REF} as a function of supply voltage at ambient temperature

The PSRR at 0 Hz was calculated as follows, based on the same simulation data as Fig. 7:

$$\text{PSRR} = 20\log\left(\frac{\Delta V_{REF}/V_{REF}}{\Delta V_{DD}/V_{DD}}\right). \qquad (17)$$

From Eq. (17), the PSRR was evaluated from a V_{DD} of 0.95 V to 1.5 V as -44 dB for both circuits.

Table III compares post-layout simulation results of the main parameters for the two proposed designs with other references found in the literature. The performance of the proposed circuits compares well to other designs except for the very low consumption in [6]. However, the circuit in [6] is based on two transistor types of different threshold voltages, which are not always available to designers.

VII. Conclusions

A MOS-only voltage reference circuit together with two different trimming methods was proposed and implemented. Both circuits operate down to a 0.95 V supply, each consuming around 4 nA. Simulations show that the circuits can be trimmed to a curvature-limited TC of 18 ppm/°C in the $-20\,^{\circ}\text{C}$ to $80\,^{\circ}\text{C}$ range. Preliminary measurements show that the circuits are functional and trimmable. More measurements will be performed to fully characterize the designs.

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References

[1] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* New York, Wiley, 2001.

[2] A. E. Buck, C. L. McDonald, S. H. Lewis, and T. R. Viswanathan, "A CMOS bandgap reference without resistors," *IEEE J. of Solid-State Circuits,*, vol. 37, no. 1, pp. 81–83, Jan. 2002.

[3] G. De Vita, and G. Iannaccone, "A Sub-1 V, 10 ppm/°C, Nanopower Voltage Reference Generator," *IEEE J. of Solid-State Circuits,* vol.42, no.7, pp.1536–1542, July 2007

[4] K. Ueno, T. Hirose, T. Asai and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE J. of Solid-State Circuits,* vol. 44, no. 7, pp. 2047–2054, July 2009.

[5] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference," *IEEE J. of Solid-State Circuits,* vol.46, no.2, pp.465–474, Feb. 2011.

[6] M. Seok, G. Kim, D. Sylvester, and D. Blaauw, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE J. of Solid-State Circuits,* vol.47, no.10, pp.2534–2545, Oct. 2012.

[7] C. Rossi-Aicardi, J. Oreggioni, F. Silveira and C. Dualibe, "A MOSFET-only voltage source with arbitrary sign adjustable temperature coefficient," *2011 IEEE NEWCAS Conf. Proc.,* pp. 366–369, June 2011.

[8] C. Rossi, C. Galup-Montoro, and M.C. Schneider, "PTAT voltage generator based on an MOS voltage divider," *Technical Proceedings of the 2007 NSTI Nanotechnology Conference and Trade Show,* Santa Clara, CA, USA, pp. 625–628, May 2007.

[9] A.I.A. Cunha, M.C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. of Solid-State Circuits,* vol. 33, no. 10, pp. 1510–1519, Oct 1998.

[10] C. Galup-Montoro and M.C. Schneider, *MOSFET Modeling for Circuit Analysis and Design,*, World Scientific Pub. Co., 2007.

[11] I.M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,*, vol.48, no.7, pp.876–884, Jul 2001.

[12] E.M. Camacho-Galeano, C. Galup-Montoro, and M.C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Trans. on Circuits and Systems II: Express Briefs,* vol. 52, no. 2, pp. 61–65, Feb. 2005.