Nanopower, Sub-1 V, CMOS Voltage References with Digitally-Trimmable Temperature Coefficient

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***Abstract*—Two variants of a MOS-only voltage reference are proposed. They are based on MOSFETs operating at a constant inversion level which cancels out non-linearities of their temperature dependence arising from that of mobility. The theory behind the circuits is thoroughly discussed, a design method is described and experimental results are presented. The two architectures propose different trimming methods for the temperature slope of the references. A test chip was designed and fabricated on a standard 0.35 μm CMOS technology including both architectures. They generate reference voltages around 710 mV, operating from 0.9 V to 3 V supply voltage while consuming 3.0 nA and 3.3 nA. The measured temperature coefficients ranged from 8 to 40 ppm/°C in the -20°C to 80°C range.**

***Index Terms*—Voltage reference, ultra low power, MOSFET, Analog integrated circuits**

I. Introduction

A VOLTAGE reference is one of the fundamental building blocks used in various devices such as A/D and D/A converters, sensor interfaces, and power management circuits. The performance of the aforementioned devices strongly depends on how constant the voltage reference maintains its output voltage with changes in supply voltage and temperature. In addition, most voltage reference designs are susceptible to random process variations. Traditional designs may also dissipate too much power for some applications such as medical implantable devices and energy-scavenging circuits, or require a supply voltage too high for a given fabrication technology.

To overcome these limitations, many voltage reference circuits have been proposed in the past: [1]–[20] are just some examples. Designs can be broadly classified in two categories: bandgap references (BGR) [1]–[7] and references based on the threshold voltage of one or more MOS transistors (VTH) [8]–[20]. Traditional BGRs produce a voltage that depends very little on process variations (near 1% [2], [6], [7]) and some of them can achieve very low temperature coefficients by compensating for second-order effects [3], [4]. However they either require resistors [1]–[4], a supply voltage higher than 1 V [2]–[6], or tend to consume more power than VTH references [7]. Resistors are usually undesirable in ultra low power designs because the needed high resistance values occupy excessive area. VTH references display a greater variability than BGRs, usually linked to the dispersion of the threshold voltage of each fabrication technology. Nevertheless, in many systems this disadvantage can be overcome, *e.g.* by digitally storing a calibration constant. Several designs have been reported [8]–[17].

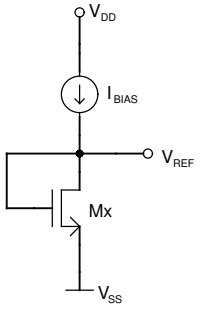

Fig. 1. Typical MOSFET-based voltage reference circuit

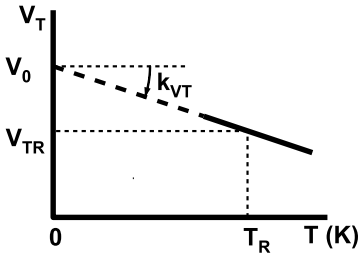

Fig. 2. Temperature dependence of the threshold voltage

The main principle for most MOSFET-only voltage references is to bias one or more MOSFETs with a current generator with some definite temperature dependence, in order to produce the reference voltage (V_{REF}). The basic topology is shown in Fig. 1 [8]. The current generator provides power supply rejection. Based on the good linearity of the threshold voltage of a MOSFET (V_T) as a function of absolute temperature (T), the obtained reference voltage is frequently equal to V_0, the extrapolation of $V_T(T)$ to 0 K (Fig. 2), which usually determines the minimum supply voltage. Some designs overcome this limitation by employing two NMOS transistors with different threshold voltages [12]–[14] but this feature

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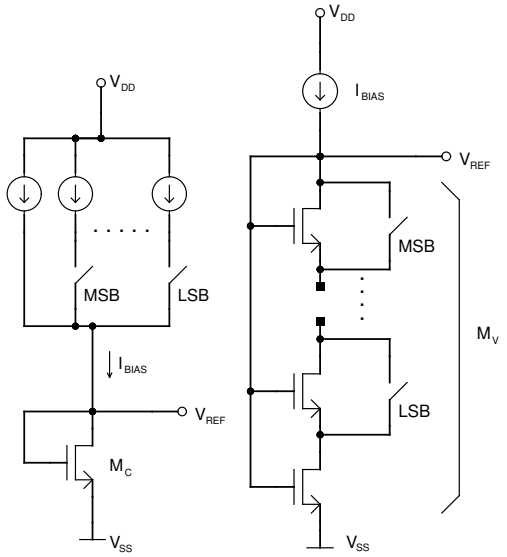


(a) Constant load (b) Variable load

Fig. 3. Simplified schematic diagrams of the proposed voltage reference architectures

is not available in all fabrication technologies. Recently, a reference based on the difference in threshold voltage in two transistors of the same type with different size was proposed [15].

The temperature dependence of a VTH reference in turn depends on the temperature dependence of the biasing current. The idea behind voltage references that exploit the particular zero temperature coefficient biasing point was originally demonstrated by Manku *et al.* [21] using a constant biasing current. A reference circuit based on this principle was presented by Filanovsky *et al.* [8]. Later Najafizadeh *et al.* [9] proposed a reference circuit using a biasing current proportional to absolute temperature (PTAT), which approximately compensates for the nonlinear temperature dependence of mobility. De Vita *et al.* [10] demonstrated a voltage reference with full cancellation of the temperature dependence of carrier mobility. The proposed current generator required NMOS transistors with two different threshold voltages. Rossi *et al.* [22] further generalized the VTH analysis for any inversion level and proposed the use of a simpler current generator, but that work only demonstrated an initial proof of concept, as no working implementation was presented. A voltage reference based on this approach was later implemented for the first time in [23]. That design requires only one type of MOS transistor and hence it is usable with any process.

This paper significantly expands the work presented in [23] by presenting a detailed design methodology, complete experimental methodology and results, together with a more comprehensive comparison with other designs in the literature. Two alternative designs are proposed as shown in Fig. 3. In both cases, a current with a particular temperature dependence biases a diode-connected MOSFET. Each design uses external digital signals to trim one of the following: (a) the biasing current or (b) the width/length ratio of the diode-connected MOSFET load. These adjustments allow the circuit to be fine-tuned to present minimal voltage variations over a large temperature range, regardless of the random process variations that affect the temperature dependence of transistor parameters. Both methods could be combined if necessary.

II. Principle of Operation

A. ACM Model

For easier reference, the following paragraphs follow [22], [24] in describing the Advanced Compact MOSFET (ACM) model [25], [26] which has been successfully applied in several of the voltage and current references in the literature [14], [20], [24], [28].

The drain current (I_D) through a long channel MOS transistor is characterized by the difference of forward and reverse currents:

$$I_D = SI_{SQ}(i_F - i_R)\,, \quad S = W/L, \tag{1}$$

where i_F and i_R are respectively the forward and reverse inversion coefficients, W, L are the effective width and length of the MOS transistor and S is called the aspect ratio. I_{SQ} is the technology-dependent sheet normalization current defined as:

$$I_{SQ} = \frac{1}{2} n\mu C_{ox} {U_T}^2\,, \tag{2}$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, n is the sub-threshold slope factor, and $U_T = kT/q$ is the thermal voltage which depends on Boltzmann's constant (k), the electron charge (q) and the absolute temperature (T). Inversion coefficients are related to transistor terminal voltages by the following close approximate equation:

$$\mathcal{F}(i_F) = \frac{1}{U_T}\left(\frac{V_G - V_T}{n} - V_S\right)\,, \tag{3}$$

where V_G and V_S are respectively the gate and source voltages referred to the bulk, V_T is the threshold voltage and $\mathcal{F}(i_F)$ is defined as [25]:

$$\mathcal{F}(i_F) \equiv \sqrt{1+i_F} - 2 + \ln\left(\sqrt{1+i_F} - 1\right)\,. \tag{4}$$

The equation for the reverse inversion coefficient (i_R) is similar to Eq. (3) using the drain voltage respect to bulk (V_D) in place of V_S.

If i_F is much larger than i_R , the transistor is considered to be operating in saturation and i_R can be neglected [25], [26]. In saturation, i_F determines the inversion level of the transistor. A rule of thumb [25] is $i_F \in$ (0,1), [1,100), [100,∞) represent weak, moderate and strong inversion respectively.

B. Voltage Reference Equations

In the proposed voltage references (Fig. 3) [22], [23], the currents that bias MOSFETs M_C and M_V make them operate at a constant inversion level. Being diode-connected, M_C and M_V operate in saturation and using (1) their current can be approximated as:

$$I_D = SI_{SQ}i_F\,. \tag{5}$$

As $V_G = V_{REF}$ and $V_S = 0$, from (3),

$$\mathcal{F}(i_F) = \frac{V_{REF} - V_T}{nU_T}. \tag{6}$$

The thermal voltage (U_T) can be written as:

$$U_T = U_{TR}\frac{T}{T_R}\ , \tag{7}$$

where U_{TR} is the thermal voltage at an arbitrary reference temperature, T_R (usually 300 K). The threshold voltage dependence with temperature is well approximated as [8] (Fig. 2):

$$V_T = V_0 + k_{VT}\frac{T}{T_R}\ , \tag{8}$$

where V_0 is the extrapolation of the threshold voltage to 0 K and k_{VT} (usually negative) is defined as:

$$k_{VT} = T_R\frac{\partial V_T}{\partial T}\ .$$

By substituting (7) and (8) into (6), the expression for the reference voltage becomes:

$$V_{REF} = V_0 + \frac{T}{T_R}\left[nU_{TR}\mathcal{F}(i_F) + k_{VT}\right]\ . \tag{9}$$

As $\mathcal{F}(i_F)$ is a strictly increasing function, Eq. (9) indicates that V_{REF} increases with temperature at high inversion levels and decreases with temperature at low inversion levels [22]. The condition for a temperature-independent V_{REF} is obtained when the second term in (9) is set to zero. This is accomplished by setting i_F such that

$$\mathcal{F}(i_F) = \frac{-k_{VT}}{nU_{TR}}\ , \tag{10}$$

thus obtaining $V_{REF} = V_0$. As the right side of this equation is constant, i_F must also be independent of temperature:

$$i_F = \mathcal{F}^{-1}\left[\frac{-k_{VT}}{nU_{TR}}\right] \tag{11}$$

where $\mathcal{F}^{-1}()$ denotes the inverse function of $\mathcal{F}()$. As this condition usually occurs at a moderate inversion level (see Section III), it is not accurate to simplify (10) with the assumption of strong inversion.

Combining (1) with $i_R = 0$ and (11) results in:

$$I_D = SI_{SQ}\mathcal{F}^{-1}\left(\frac{-k_{VT}}{nU_{TR}}\right)\ . \tag{12}$$

It is worth stressing that I_D is proportional to I_{SQ} (in turn proportional to $\mu(T)U_T^2$) and thus not constant with temperature. This current is easily achieved with the bias generator described in Section III-A.

The constant inversion coefficient condition imposed by the particular bias generator cancels the non-linear temperature dependence stemming from mobility [22]. Only the almost linear temperature dependence originated in the threshold voltage remains which is compensated by a scaled thermal voltage U_T. The scaling is controlled through the inversion coefficient i_F. Due to process variations, k_{VT} can not be accurately predicted and hence i_F must be trimmed to compensate for variations. From (5) there are two possible ways to trim i_F: (a) adjust I_{BIAS} or (b) adjust S in M_V, as illustrated in Fig. 3. Both of these architectures are explored in this work.

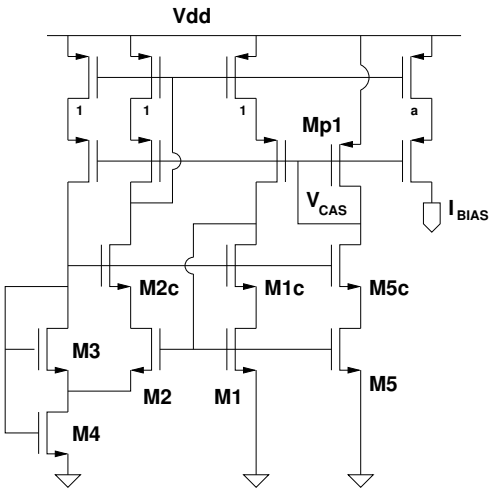


Fig. 4. Schematic diagram of the constant inversion level current source

III. Circuit Design

A. Constant inversion level current source

As the voltage reference circuits in Fig. 3 require currents with a constant inversion coefficient i_F, independent of temperature, the design of a block delivering such currents will be detailed first [24], [28], [29]. A schematic of the current source used in this work is shown in Fig. 4. The core of this source is composed by transistors M_1–M_4. The PMOS transistors implement a high-swing cascode current mirror for improved power supply rejection and reduced systematic error due to finite output conductances. An additional current branch (M_{p1}, M_{5c} and M_5) is required to generate V_{CAS} [27]. The gains of the PMOS mirror are shown in the figure. Transistors M_{1c}, M_{2c} and M_{5c} act as cascodes for M_1, M_2 and M_5, respectively. The bulk contact is grounded for all NMOS and connected to V_{dd} for PMOS transistors. The currents in the four core transistors satisfy:

$$I_{D1} = I_{D2} = I_{D3} = \frac{1}{2}I_{D4}\ . \tag{13}$$

Neglecting variations of n and μ with V_G and assuming uniform temperature across the circuit, I_{SQ} is the same for all NMOS transistors, thus from (1) it follows:

$$S_1 i_{F1} = S_2 i_{F2} = S_3 i_{F3} = \frac{1}{2}S_4(i_{F4} - i_{F3})\ , \tag{14}$$

since M_1, M_2, M_3 are saturated and $i_{F3} = i_{R4}$ which results from (3) with $V_{G3} = V_{G4}$ and $V_{S3} = V_{D4}$. Also, $V_{G1} = V_{G2}$, together with $V_{S1} = 0$, imply (3):

$$\mathcal{F}(i_{F2}) = \mathcal{F}(i_{F1}) - \frac{V_{S2}}{U_T}\ , \tag{15}$$

and since $V_{G3} = V_{G4}$, then:

$$\mathcal{F}(i_{F3}) = \mathcal{F}(i_{F4}) - \frac{V_{S2}}{U_T}\ . \tag{16}$$

From (15) and (16),

$$\mathcal{F}(i_{F1}) - \mathcal{F}(i_{F2}) = \mathcal{F}(i_{F4}) - \mathcal{F}(i_{F3})\ . \tag{17}$$

Equations (14) and (17) completely determine the inversion coefficients of all NMOS transistors as a function of their aspect ratios. Thus, the circuit produces a bias current exactly proportional to I_{SQ}. The inversion coefficients (i_{F1}, i_{F2}, i_{F3} and i_{F4}) are independent of technology parameters, voltage supply, and temperature [22], [24]. The generated current is as follows:

$$I_{BIAS} = a\,(S_2 i_{F2} I_{SQ}) \ , \tag{18}$$

where a is the gain of the output branch of the PMOS current mirror and I_{SQ} depends on temperature through $\mu(T)$ and U_T.

In this work, the methodology to determine the aspect ratio of NMOS transistors differs from the one proposed in [28], which restricts operation to moderate and weak inversion. The design method begins by setting a target I_D and weak inversion levels for M_1 and M_2. For low sensitivity to process variations, i_{F1} must be several times higher than i_{F2}. M_3 usually operates in moderate or strong inversion, thus i_{F3} is set to many times i_{F1} considering that the greater this value, the design becomes more robust but also the required area increases. Using this value in Eq. (17), i_{F4} is found. Finally, S_1, S_2, S_3 and S_4 are determined from Eq. (14). For good matching, M_1 to M_4 and the diode connected load MOSFETs (M_C, M_V) are designed as series or parallel combinations of the same unit transistor M_U.

To adjust the inversion level in M_C (i_{FC}), a is trimmable in the architecture of Fig. 3(a):

$$i_{FC} = a\frac{S_2 i_{F2}}{S_C} \ , \tag{19}$$

where S_C is the aspect ratio of M_C. The inversion level in M_V (Fig. 3(b)) is controlled by adjusting its channel length (L_V) while keeping a constant:

$$i_{FV} = \frac{1}{S_V} a S_2 i_{F2} = L_V \frac{a S_2 I_{F2}}{W_V} \ , \tag{20}$$

where i_{FV}, S_V and W_V denote the forward inversion coefficient, the aspect ratio and the channel width of M_V, respectively.

B. Range and resolution of trimming

As stated in Section II-B, the inversion coefficient (i_F) of the diode-connected MOSFET (M_C or M_V) must be trimmed to approximate the condition of temperature independence (10). Therefore, the range and resolution of such trimming must be assessed. With α_T defined as the derivative of V_{REF} with respect to temperature, differentiating (9) results in

$$\alpha_T \equiv \frac{\partial V_{REF}}{\partial T} = \frac{1}{T_R}\left(n U_{TR} \mathcal{F}(i_F) + k_{VT}\right) \ . \tag{21}$$

It must be noted that setting $\alpha_T = 0$ in (21) leads to (11). Neglecting the small temperature dependence of n, the required range of i_F ($i_{F_{MIN}}$ to $i_{F_{MAX}}$) is determined by the dispersion of k_{VT} due to process variations. Thus, the range of i_F needed to ensure trimmability is determined by the range of k_{VT} through (11).

As i_F is trimmed in discrete steps (Δi_F), α_T cannot be made exactly equal to zero and it will be bounded by a design specification $\alpha_{T,MAX}$ so that $|\alpha_T| < \alpha_{T,MAX}$. Fig. 5 shows

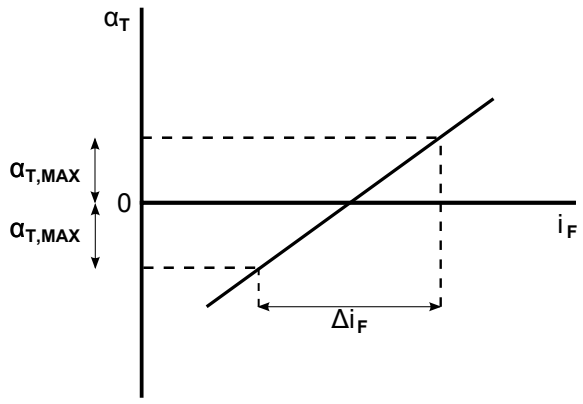


Fig. 5. Temperature slope of reference voltage *vs.* inversion coefficient

α_T *vs.* i_F near $\alpha_T = 0$. From the figure it is clear that the trimming step Δi_F must be chosen so that

$$\Delta i_F < \frac{2\alpha_{T,MAX}}{\left.\frac{d\alpha_T}{di_F}\right|_{\alpha_T=0}} \tag{22}$$

is fulfilled for any k_{VT} in its dispersion range. This is guaranteed in the worst case if

$$\Delta i_F \le \frac{2\alpha_{T,MAX}}{\left.\frac{d\alpha_T}{di_F}\right|_{MAX}} \le \frac{2\alpha_{T,MAX}}{\left.\frac{d\alpha_T}{di_F}\right|_{\alpha_T=0}} \ . \tag{23}$$

The worst case slope is calculated from (21) as

$$\left.\frac{d\alpha_T}{di_F}\right|_{MAX} = \frac{nU_{TR}}{T_R} \cdot \left.\frac{d\mathcal{F}(i_F)}{di_F}\right|_{MAX} \ ; \tag{24}$$

where, from (4),

$$\left.\frac{d\mathcal{F}(i_F)}{di_F}\right|_{MAX} = \frac{1}{2}\frac{1}{\sqrt{1+i_{F_{MIN}}}-1} \ . \tag{25}$$

Combining (23), (24) and (25), the maximum acceptable Δi_F is:

$$\Delta i_F \le \frac{4\,T_R\,\alpha_{T,MAX}\,\left(\sqrt{1+i_{F_{MIN}}}-1\right)}{n\,U_{TR}} \ . \tag{26}$$

From (5) and $S = W/L$,

$$i_F = \left(\frac{1}{W I_{SQ}}\right) I_{BIAS} L \ . \tag{27}$$

In the constant load architecture [Fig. 3(a)], I_{BIAS} is trimmed in ΔI_{BIAS} steps while in the variable load architecture [Fig. 3(b)] the length L of M_V is trimmed in ΔL steps. From (27) it follows that both ΔL and ΔI_{BIAS} are proportional to Δi_F.

The switches depicted in Fig. 3 are implemented with transistors. These trimming transistors are arranged in a bit-wise manner, with the least-significant-bit (LSB) producing the smallest change of i_F (Δi_F) and each successive bit increasing the change by powers of two adjusting length or current depending on the architecture. Once the range and resolution of i_F are established, the required number of bits can be determined from:

$$\frac{i_{F_{MAX}} - i_{F_{MIN}}}{\Delta i_F} \le 2^N - 1 \ , \tag{28}$$

where N is the number of bits as well as the number of trimming switches. If a single unit transistor M_U is used to implement the LSB in the variable load architecture, the number of unit transistors in M_V is

$$N_T = \frac{i_{F_{MAX}}}{\Delta i_F} \ . \tag{29}$$

C. Biasing Strategy

In both architectures, the consumption is determined by the bias current. The minimum I_{BIAS} is constrained by the errors introduced by currents leaking to substrates in reverse-biased drain/source junctions (I_{LEAK}) and by the off-state currents through the switch transistors (I_{OFF}). Both kinds of current increase with temperature and their values at the maximum operating temperature T_{MAX} are considered here.

The total effect of these error currents on V_{REF} should be ideally much less than $\alpha_{T,MAX}(T_{MAX} - T_{MIN})$, or at most comparable to this value. Thus, the maximum deviation in the inversion coefficient due to these error currents should be less than Δi_F as computed from (26) and the following condition is imposed on I_{BIAS}:

$$\frac{\sum I_{LEAK_{MAX}} + \sum I_{OFF_{MAX}}}{I_{BIAS}} \leq \frac{\Delta i_F}{i_{F_{MAX}}} \ . \tag{30}$$

In the variable load circuit [Fig. 3(b)], the involved error stems from leakage in M_V and in the fixed current source as well as from off-state currents in the switches that trim M_V, while in the constant load architecture [Fig. 3(a)], the involved error currents are leakage and off-state currents in the variable PMOS current mirror and leakage currents in M_C. It must be noted that $\sum I_{LEAK_{MAX}}$, in turn, depends mainly on the number of unit transistors in the diode-connected M_V or M_C.

D. Design Summary

A test circuit that implements both architectures shown in Fig. 3 was designed and fabricated on a standard 0.35 μm CMOS technology. The design choices are outlined in Table I.

TABLE I
DESIGN VALUES AND CHOICES

α_T	3.65 $\mu V/K$ (*)
i_F Range	37 to 59
N	6 bits
I_{D2} [Fig. 4]	0.6 nA
I_{DC} [Fig. 3(a)]	1 nA to 1.6 nA
I_{DV} [Fig. 3(b)]	1.2 nA
Design Consumptions:	
Current Source	2.1 nA
Constant Load circuit	3.1 to 3.7 nA
Variable Load circuit	3.3 nA

(*) 5 ppm/K @ V_0 = 730 mV

It should be noted that the range of inversion coefficients, which depends only on technology parameters (11), corresponds to moderate inversion. This fact confirms that the analysis and design of this circuit must be based on a model of the MOS transistor that is valid through all operating regions.

TABLE II
NMOS TRANSISTOR SIZES

M_U	1 μm / 24.9 μm
M_1, M_2, M_3, M_4 [Fig. 4]	2(P), 16(P), 20(S), 22(S)
M_C [Fig. 3(a)]	130(S)
M_V [Fig. 3(b)], {MSB, ...,LSB}	106(S), {32(S), 16(S), 8(S), 4(S), 2(S), 1}

Table II shows the resulting NMOS transistor dimensions. M_C in Fig. 3(a), M_V in Fig. 3(b) and M_1 to M_4 in the constant inversion level current source are composed with series or parallel combinations of the same unit transistor M_U. 'S' and 'P' indicate that the unit transistors are connected in series or parallel, respectively.

The constant inversion level current source consumes 3.5 times its branch current I_{D2}. This includes a reduced current auxiliary branch used to bias the PMOS cascodes. The output branch for the variable load doubles the branch current ($a = 2$) and the output for the constant load is trimmable from $a = 5/3$ to $a = 5/3 + 63/64$. Thus, regarding design values, a complete variable load circuit would consume $(3.5 + 2) \times 0.6$ nA $=$ 3.3 nA. In a similar way, a complete constant load circuit would consume 3.1 nA to 3.7 nA depending on the trimming value.

The NMOS portion of the layout is depicted in Fig. 6. Both architectures as well as the shared current source are included in the same transistor array and are surrounded by dummy transistors. The trimming switches are controlled through an on-chip shift register in order to decrease the pin count. A microphotograph of the fabricated die including the I/O pads is shown in Fig. 7. The dimensions are 74.55 μm x 184.30 μm $\cong$ 0.014 mm^2 for the PMOS block and 433.00 μm x 226.45 μm $\cong$ 0.098 mm^2 for the NMOS block. The area for a complete constant load circuit [Fig. 3(a)] is approximately 0.054 mm^2 and that for a complete variable load circuit [Fig. 3(b)] is approximately 0.068 mm^2.

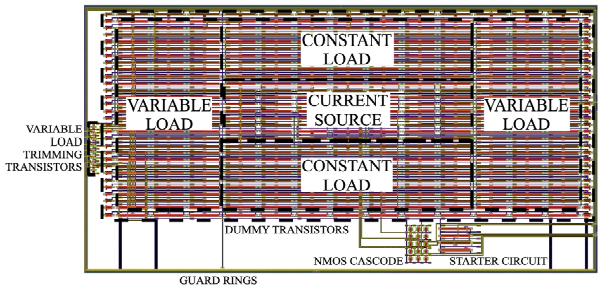


Fig. 6. Overview of the layout of the NMOS block

IV. EXPERIMENTAL RESULTS

A. Temperature dependence (before trimming)

The temperature dependence of both architectures was evaluated from -20°C to 80°C. Measurements in the range from $-20°$ C to 20° C were performed using a temperature-controlled laboratory refrigerator, while the range from 30° C to 80° C was measured with a temperature-controlled oven.

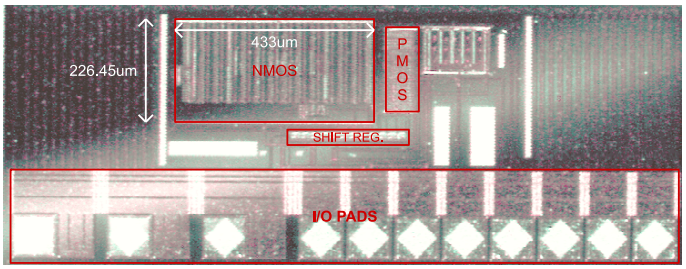
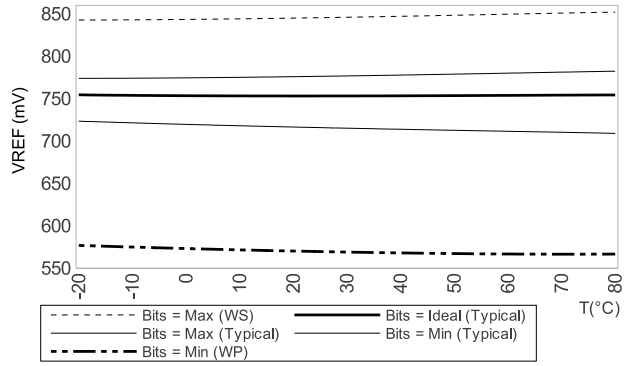
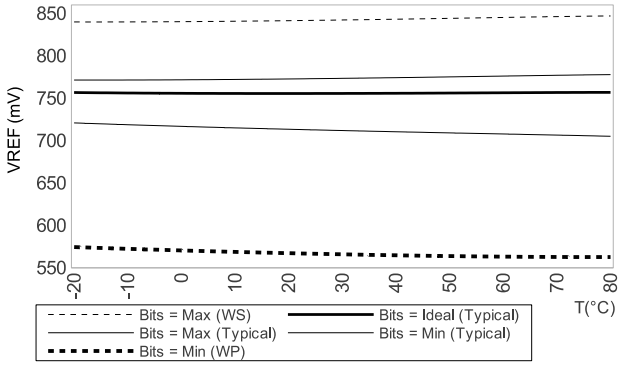


Fig. 7. Microphotograph of the fabricated chip

The supply voltage V_{DD} was kept fixed at 1.5 V, well within the operational range of the circuit, both for simulations and measurements.



(a) Constant load



(b) Variable load

Fig. 8. Simulated output voltage as a function of temperature at different trimming levels and process corners

Simulation results of the output voltage as a function of temperature at different trimming values and process corners are shown in Fig. 8. The dotted plots correspond to the extreme combinations of trimming and process corners representing the whole range of voltages that may be expected. Also shown in Fig. 8 is the output voltage for a typical process with all configuration bits set for maximum output (Bits = 63, $i_{F_{MAX}}$) and minimum output (Bits = 0, $i_{F_{MIN}}$). In the first case the output voltage had an average positive slope with respect to temperature, while in the latter the average slope was negative as predicted by (9). This shows that it is possible to trim both circuits to a temperature slope close to zero.

A Monte Carlo sampling analysis with 1000 untrimmed samples was performed. The mean and standard deviation for the output voltages are summarized in Table III. The standard deviation is high but it would be reduced to the standard deviation of V_0 for the fabrication process after trimming. Fig. 9 shows histograms for the temperature coefficient defined

TABLE III
UNTRIMMED OUTPUT VOLTAGE STATISTICS FOR 1000 MONTE CARLO SAMPLES

	Constant Load	Variable Load
mean (mV)	754	756
standard deviation (mV)	87	87

as:

$$TC = \frac{1}{V_{REF_{AVG}}} \left[\frac{V_{REF_{MAX}} - V_{REF_{MIN}}}{T_{MAX} - T_{MIN}} \right] . \qquad (31)$$

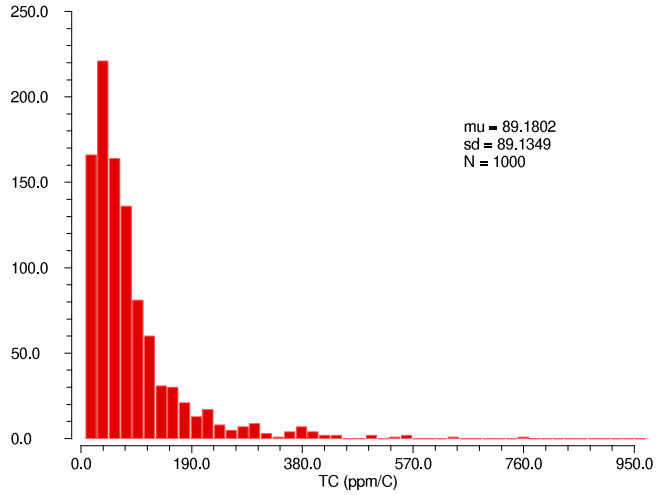
when both process variations and mismatches are considered. The TC for most samples can be reduced to acceptable levels by trimming, but some samples have unacceptably high values that can not be trimmed. Further investigation shows that if only process parameter variations are considered, the mean values are reduced to 22.9 ppm and 22.0 ppm for the constant and variable loads, respectively. The corresponding worst-case TC values are reduced to 54 ppm and 50 ppm, respectively. This indicates that the main cause for low performance is mismatch. That is a shortcoming of this implementation and is probably caused by too small unit transistors in the PMOS current mirror (branch with minimum area has two units with 2 μm^2 each). Thus, the determination of the trimming range should also consider mismatch effects in addition to k_{VT} dispersion.

For each architecture, V_{REF} was measured at several temperatures in the $-20°$ C to $80°$ C range while the trimming bits were programmed at both ends of the trimming range. Results for Sample #2 are shown in Fig. 10. As expected, the measurements increase or decrease (depending on the trimming value) quite linearly with temperature, which is consistent with theoretical and simulation results.

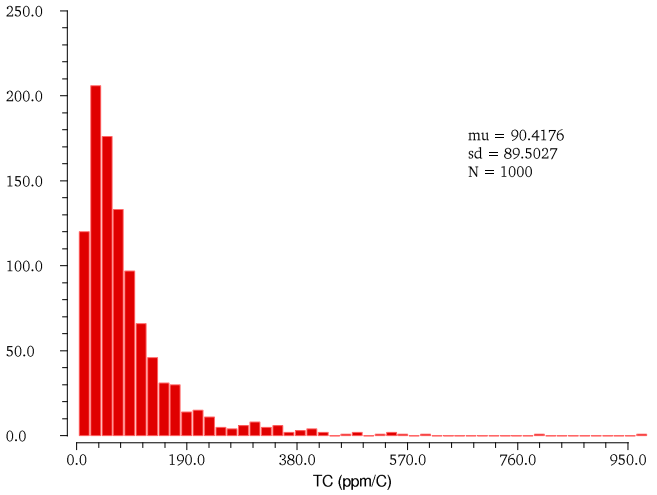
B. Trimming method

The extrapolation of the straight lines that best fit the measurements in Fig. 10 intersect approximately at $T = 0\ K$ and the corresponding voltage is $\hat{V}_0$, which is an estimation of V_0 in (8). The measured steps in output voltage when switching each trimming bit are shown in Fig. 11 for ambient temperature. These steps are only approximately proportional to the weight of each bit due to the slight nonlinearity in the considered interval of $\mathcal{F}(i_F)$.

All samples of the variable load architecture worked as expected with the weight approximately doubling for each consecutive bit. That was not the case with some of the samples of the constant load architecture. This problem resulted in a lower calibration resolution for the affected samples.

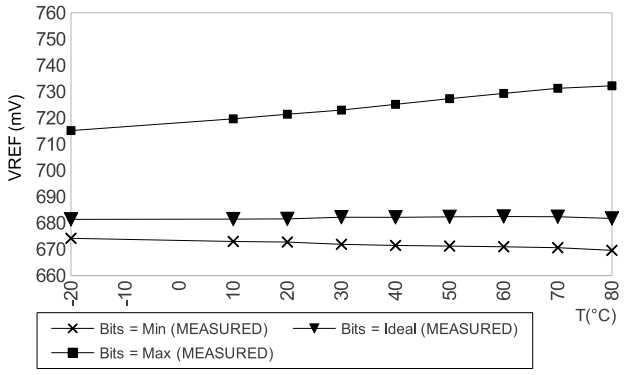


(a) Constant load

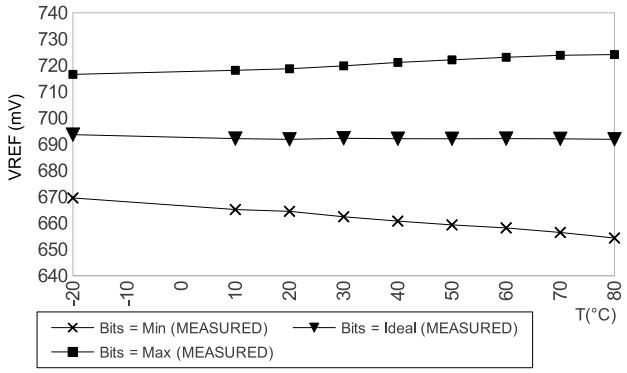


(b) Variable load

Fig. 9. Untrimmed temperature coefficient histograms for 1000 Monte Carlo samples



(a) Constant load



(b) Variable load

Fig. 10. Measured output voltage *vs.* temperature, extreme and optimal trimmings for Sample #2

Since the output voltage at ambient temperature must be equal to V_0, the value of $\hat{V}_0$ determined from Fig. 10, along with the least significant bit step (ΔV) provide a means to experimentally find the bit combination required for a temperature slope close to the minimum one through:

$$\text{Trim} = \frac{\hat{V}_0 - V_{out,MIN}}{\Delta V} , \tag{32}$$

where Trim is the binary number formed by the trimming bits, $V_{out,MIN}$ is the output voltage for minimum trim. In this work $V_{out,MIN}$ and ΔV were both measured at ambient temperature. ΔV can be directly measured (Fig. 11) or can be estimated as follows:

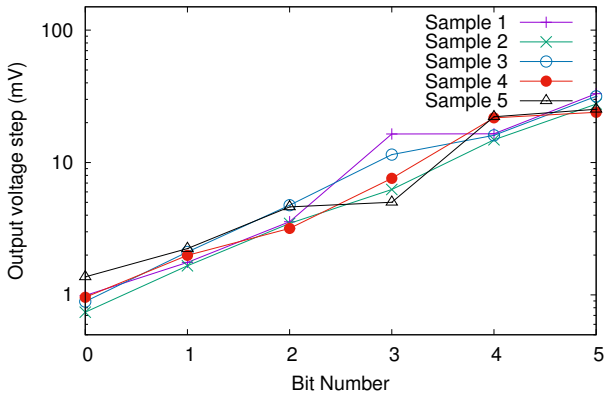
$$\Delta V = \frac{V_{out,MAX} - V_{out,MIN}}{64} ,$$

where $V_{out,MAX}$ is the output voltage for maximum trim. Although not optimum, this rough but practical trimming method proved to be quite appropriate as will be shown further on. This method also has the advantage of not requiring the characterization of process parameters values for each sample. For a quick calibration, it is possible to obtain the trim of a chip with just three measurements: $V_{out,MAX}$ and $V_{out,MIN}$ at room temperature to determine ΔV and $V_{out,MAX}$ (or $V_{out,MIN}$) at a different temperature to find $\hat{V}_0$.

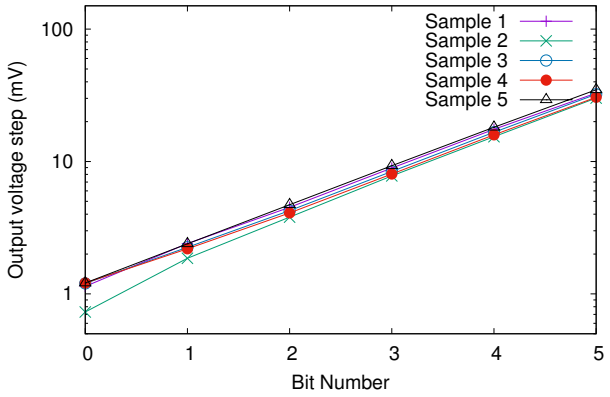
C. Temperature dependence (after trimming)

After trimming, the output voltage for each architecture was measured at different temperatures as depicted in Fig. 12 while the variations of V_{REF} respect to its value at 20°C are shown in Fig. 13. The average measured output voltages through the temperature range $V_{REF_{AVG}}$ are shown in Table IV together with estimated consumption (I_{DD}), trimming values and residual temperature coefficient (TC). The Trim column is the 6-bit combination value (as a binary number) computed with (32). All bits turned off corresponds to 0 while all bits turned on corresponds to 63.

The trimming values for Sample 4, constant load, and Sample 5, both architectures, are either the maximum or minimum possible ones. This is an indication that the necessary trimming range was underestimated as a consequence of underestimating the mismatch effects and lacking a good characterization for the range of k_{VT} in (8). Therefore, residual temperature coefficients are rather high in those cases. Also, the variation of V_{REF} across different samples is approximately 86 mV in the worst case. These variations are within the expected range

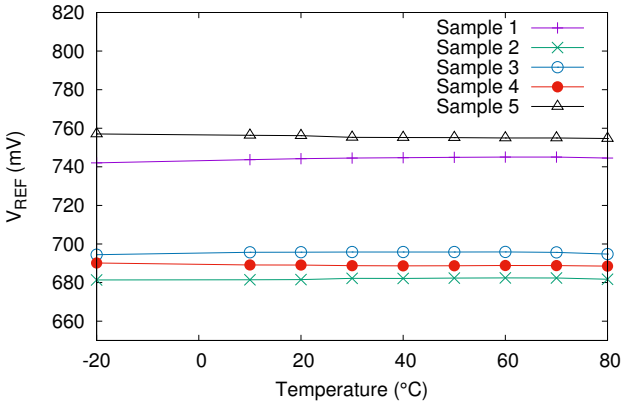


(a) Constant load

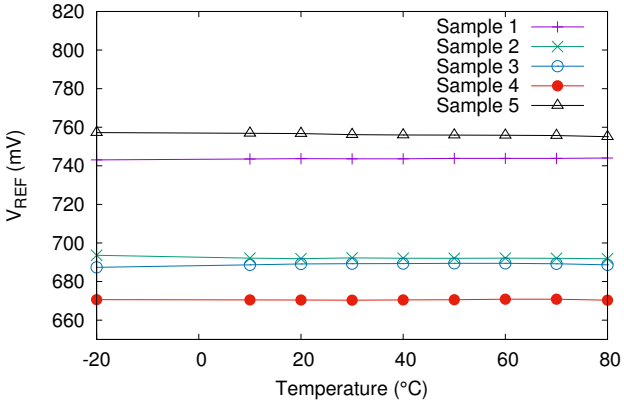


(b) Variable load

Fig. 11. Measured output voltage step for each trimming bit at room temperature



(a) Constant load



(b) Variable load

Fig. 12. Measured trimmed output voltage as a function of temperature

TABLE IV
SUMMARY OF MEASUREMENT RESULTS

Sample	Trim	$V_{REF_{AVG}}$ (mV)	TC (ppm/°C)	I_{DD} (*) (nA)
	Constant Load			
1	32	744.3	40	2.8
2	12	682.0	16	1.8
3	16	695.5	21	2.4
4	0	689.0	23	2.3
5	63	755.3	31	3.3
	Variable Load			
1	45	743.7	14	2.7
2	30	692.2	26	1.8
3	8	689.0	31	2.5
4	10	670.6	8	2.4
5	63	756.2	28	3.0

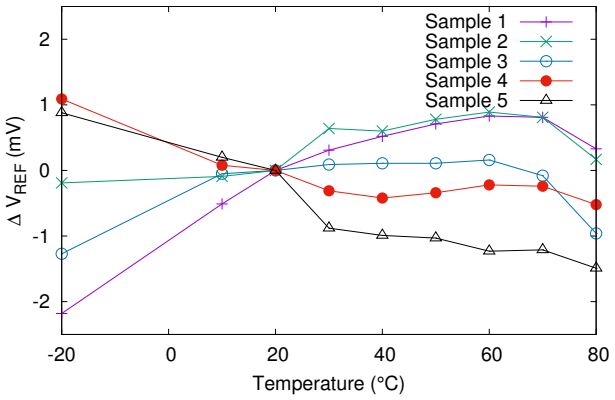
(*) @$V_{DD} = 3.0\ V$

for process corners and constitute a limitation of many VTH references. It would be expected that the values of $V_{REF_{AVG}}$ for both architectures on the same chip to be equal as they are ideally the threshold voltage extrapolated to zero Kelvin (V_0). With sufficient matching in the layout, the transistors should have very similar threshold voltages. These were compared in the correctly trimmed samples (1, 2 and 3) and the residual mismatch was better than 10.2 mV. Reference voltages ranging approximately from 670 mV to 756 mV were obtained, each varying slightly over ± 2 mV in the -20°C to 80°C range.

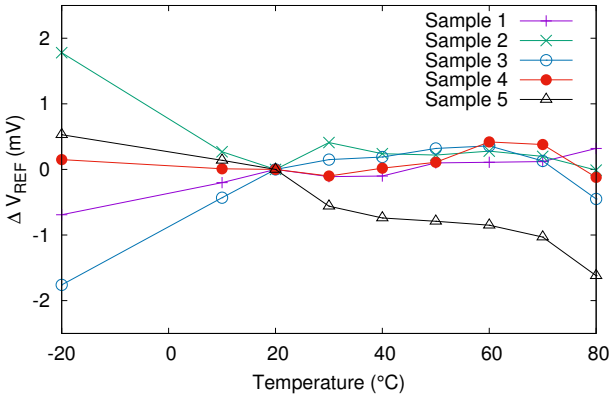
As only five samples were available for measurement, it is not possible to calculate a meaningful value for the average and the standard deviation of measured parameters [30]. However, five samples are enough to conclude with a probability of 93% that the median for the TC is within the intervals defined by the measured values: 8.1 ppm/°C to 30.8 ppm/°C and 15.8 ppm/°C to 40.5 ppm/°C for the variable and constant load architectures, respectively.

D. Consumption

Both architectures depend on the constant inversion level bias current generated in the circuit in Fig. 4 for working as designed. The simulated and measured reference current



(a) Constant load



(b) Variable load

Fig. 13. Variations in trimmed output voltage with respect to the voltage at 20°C as a function of temperature

(I_{D2}) as a function of the supply voltage V_{DD} is shown in Fig. 14. As expected, the dependence with V_{DD} is low. All of the measured currents are smaller than the current predicted by simulation with typical process parameters, but they are within the range predicted by Monte Carlo simulations. As both designs are independent of the process-dependent sheet normalization current, voltage outputs for all measured chips behave as expected, as already shown in Fig. 12 and Fig. 13.

From these measurements of I_{D2} and assuming the PMOS mirror current ratios as discussed in section III-D, the experimental consumption of each architecture can be estimated from data in Fig. 14. These estimations were performed at $V_{DD} = 3.0\ V$ which corresponds to the maximum measured reference current for each sample. In the case of constant load circuits, the current ratio of the mirror was chosen for each sample to match the trimming value from (32). The results are shown in Table IV. For the constant load architecture the estimated consumption range is 1.8 nA to 3.3 nA while in the case of variable load the estimated consumption lies between 1.8 nA and 3.0 nA.

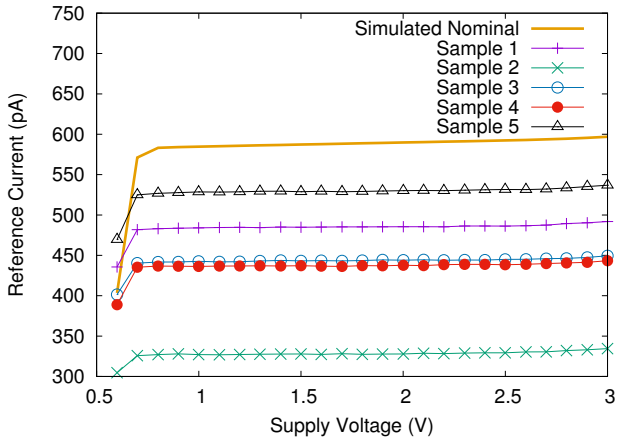


Fig. 14. Reference current as a function of supply voltage

E. Voltage supply dependence

The scarce dependence of V_{REF} with V_{DD} through a wide range of supply voltage is shown in Fig. 15. Two voltages are shown for each sample, the lowest was obtained by setting all trimming bits to '0' and the highest was obtained by setting all bits to '1'.

The line sensitivity (LS) was evaluated at ambient temperature using data from Fig. 15 with V_{DD} ranging from 0.9 V to 3 V using the following equation:

$$LS = \frac{\left(\frac{V_{REF_{MAX}} - V_{REF_{MIN}}}{V_{DD_{MAX}} - V_{DD_{MIN}}}\right)}{V_{REF_{MIN}}} \times 100\% \ . \qquad (33)$$

TABLE V
MEASURED LINE SENSITIVITY

Sample	Variable Load		Constant Load	
	Bits: Min (%/V)	Bits: Max (%/V)	Bits: Min (%/V)	Bits: Max (%/V)
1	0.15	0.26	0.14	0.22
2	0.17	0.19	0.14	0.17
3	0.13	0.16	0.12	0.30
4	0.13	0.18	0.12	0.14
5	0.14	0.20	0.14	0.20

Table V shows the line sensitivity for each combination of sample and architecture in the extreme trimmings.

F. Noise Performance

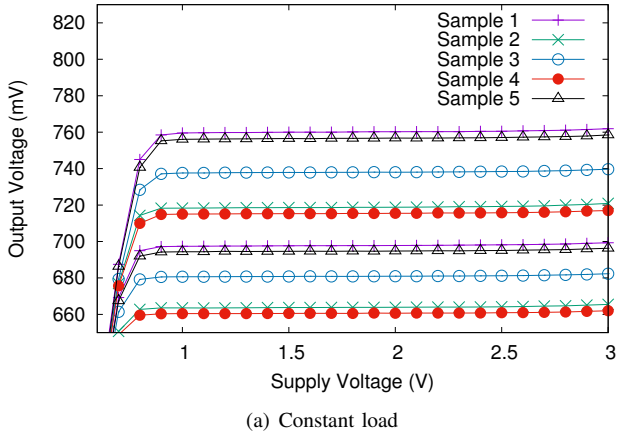
The simulated noise spectral density without filtering capacitors for the two architectures is shown in Fig. 16. Noise in this design is relatively high due to the low currents. The total integrated noise for the constant load architecture is 0.20 mV_{RMS} and for the variable load is 0.17 mV_{RMS}.

V. Comparison with other designs

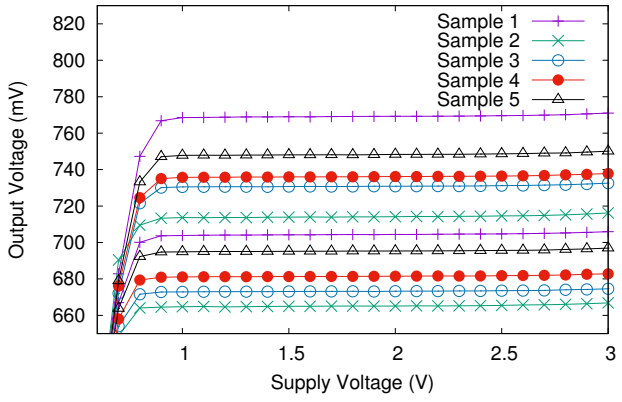
Table VI compares the experimental results of the two proposed designs with other published voltage references that include experimental results. The designs in the literature have been classified in three categories: BGR with no resistors, MOSFET-only designs, and other designs. The work in [18] is

TABLE VI
COMPARISON OF EXPERIMENTAL RESULTS WITH PREVIOUS RESEARCH

	This work		BGR (no R)		MOSFET only							Other		
	Const. Load	Var. Load	[6]	[7]	[10]	[11]	[12]	[13]	[14]	[15]	[17]	[2]	[18]	[19]
Technology (μm)	0.35	0.35	0.18	0.13	0.35	0.35	0.18	0.13	0.18	0.18	0.18	0.09	0.35	0.18
Supply Voltage (V)	0.9–3	0.9–3	0.7–1.8	0.5–1.5	0.9–4	1.4–3	0.45–2	0.5–3.0	0.8–3.6	0.15–1.8	0.45–1.8	1.2	1.9–3.3	0.7–1.8
Consumption (nA)	3.3	3.0	75	64	40	214	5.8	0.059	106	0.174	34.7	480	65×10^3	27
V_{REF} (mV)	713	710	548	498	670	745	257.5	176	400	17.7	118.4	720	905.5	438.7
$\sigma(V_{REF})$ (mV)	87.2	87.3	8.9	3.3	21	60	10	0.32		0.29	0.69	6.3		
LS (%/V)	0.30	0.26			0.27	0.002	0.440	0.036		2.03	0.033	0.3		0.13
TC (ppm/°C)														
Average	26	21	114			15	165	29	14.6	1462.4	59.4	53.1		22.11
Best	16	8		75	10	7	39	5.3			25	43.5	14.8	
Worst	40	31		125		45	357	47.4			240	60.7	25.3	
Measured samples	5	5	9	6	20	17	40	30	9	60	50	5	5	40
Range (°C)	[-20, 80]	[-20, 80]	[-40, 120]	[0, 80]	[0, 80]	[-20, 80]	[0, 125]	[-20, 80]	[-40, 80]	[0, 120]	[-40,85]	[0, 100]	[0, 100]	[-25, 85]
Trimmed	Yes	Yes	No	Yes	No	No	No	Yes	Yes	Yes	Yes	No	Yes	Yes
Area (mm^2)	0.054	0.068	0.0246	0.0264	0.045	0.055	0.043	0.0093	0.00135	0.0012	0.0132	0.028	0.01	0.041



(a) Constant load



(b) Variable load

Fig. 15. Measured maximum and minimum output voltages as a function of supply voltage

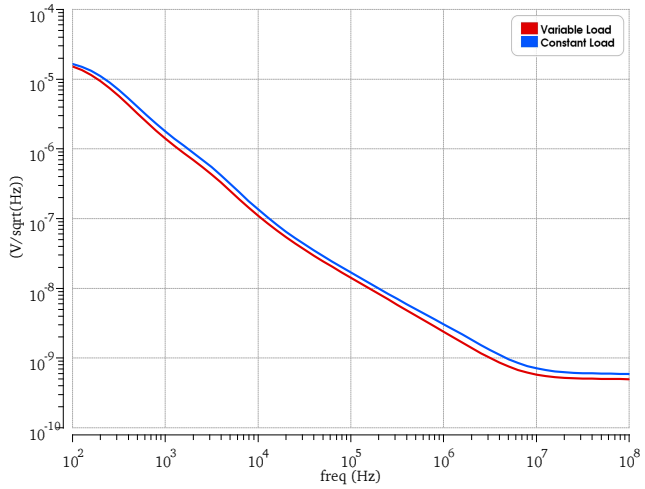


Fig. 16. Output noise power spectral density

a VTH reference but requires two BJT, and [2], [19] are BGR with resistors but they are included in this comparison because their consumption is low and they require a small area.

The consumptions reported in Table VI for this work correspond to the worst cases in Table IV; the reference voltage values are the averages of those in Table IV for each architecture; values for line sensitivity (LS) are the worst cases in Table V while those of temperature coefficients (TC) are the average, best and worst cases from Table IV.

The performance of the proposed circuits is comparable to the other designs reported in the literature except for the large standard deviation of the reference voltage ($\sigma(V_{REF})$). The value reported in the table is very pessimistic obtained from 1000 untrimmed Monte Carlo samples. If the measured values are used, the corresponding $\sigma(V_{REF})$ for the constant and variable load are reduced to 30.4 mV and 33.4 mV, respectively, which is within the V_0 process variation range. These values are comparable to the values reported in [10]–[12]. The current consumption is the lowest among all circuits except [13] and [15]. However, the TC and LS performances are poor in [15], while the circuit in [13] along with [10], [12], [14] are based on two transistor types with different threshold voltages, which are not always available to designers or well characterized. Among all of the circuits compared in the table, only the proposed ones and [11], [15] are implemented exclusively with standard MOSFETs in a common substrate with a single threshold voltage.

In terms of area the proposed designs are competitive when the low current consumption is considered. The exception is [13], which uses an exceptionally low current with low area.

VI. Conclusion

Two MOS-only voltage references suitable for low voltage and ultra low power applications were presented. They require only one type of NMOS and PMOS transistors, no BJTs and no resistors and hence are usable with any CMOS process.

A detailed theoretical modelling and the resulting design method, both based on ACM, allowed to achieve an optimized design even though the circuits operate in moderate inversion

The constant inversion level bias current produces a very linear residual temperature dependence of the reference voltage through compensation of the nonlinear temperature dependence of mobility. Both trimming methods proved to be effective to compensate the linear temperature dependence related to the threshold voltage. Simulation results indicate that mismatch effects are as important as k_{VT} dispersion for the determination of the trimming range.

A test chip was fabricated in a standard 0.35 μm CMOS technology and extensively measured. Both circuits operate down to a 0.9 V supply and generate a reference voltage around 710 mV. The variation of the reference voltage across different samples was at most 86 mV. The circuits consume 3.0 nA and 3.3 nA with line sensitivity of at most 0.30 %/V. The experimental temperature coefficient in the $-20°$C to $80°$C range was less than 40 ppm/°C, with the best performance at 8 ppm/°C. The areas are 0.054 mm^2 and 0.068 mm^2.

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