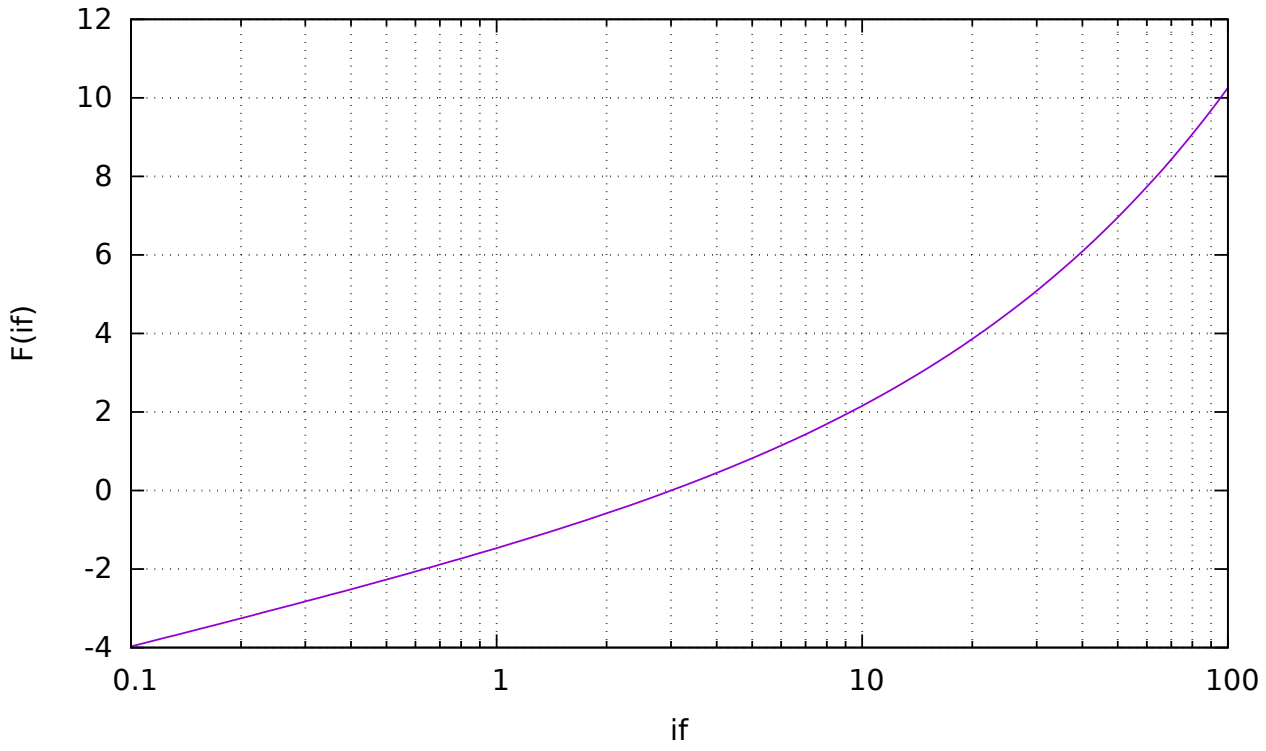
ENGI 5131 Microelectronics
Final Exam — Winter 2017

ACM parameters for all problems:

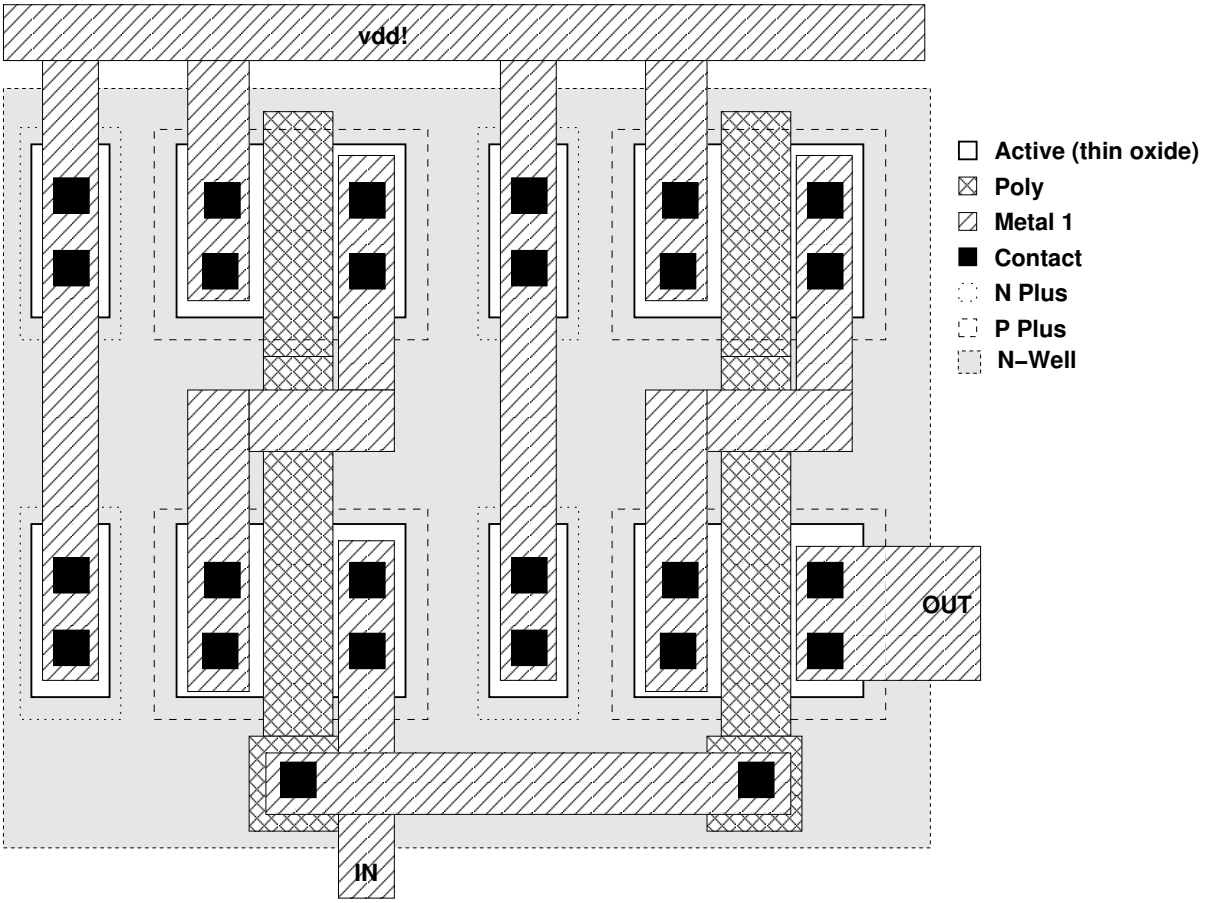
	N-channel	P-channel
V_{th} (V)	0.39	-0.41
I_{SQ} (nA)	110	35
n	1.3	1.3
$\lvert\partial L/\partial V_{DS}\rvert$ (μm/V)	0.05	0.05
L_D (nm)	20	20

- Consider L_D for short channels
- Show calculation steps
- Make reasonable assumptions for any missing data.



Problems and Questions

1. The following layout is for a process with p-type substrate. Draw an schematic diagram of the circuit in this layout. Show transistor substrate connections and node labels in the schematic.



2. For an inverter with $L = 0.2\ \mu$m for both transistors and $W_n = 0.6\ \mu$m, estimate W_p for a threshold voltage equal to 1.1 V with a supply voltage of 1.6 V. Neglect short-channel effects.

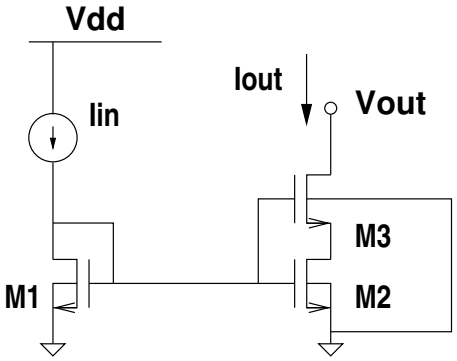
3. All three transistors in the figure are equal with $W = 70$ μm and $L = 1.5$ μm. The input current is $I_{IN} = 5$ μA.

   (a) Calculate the forward and reverse inversion levels in M2 and M3, assuming V_{OUT} is 1 V.

   (b) Calculate the output current (I_{OUT}).

   (c) Calculate the minimum value of V_{OUT} that keeps the output current regulated.

   (d) Calculate the percentage change in output current if V_{OUT} changes by 1 V.



4. The differential amplifier shown in the figure has been designed to operate as follows: $i_{f1} = i_{f2} = 20$, $i_{f3} = i_{f4} = 80$, $i_{f5} = 150$. Assume all transistors have $L = 2$ μm. Other circuit parameters: $V_{DD} = 1.8$ V, $C_L = 0.5$ pF.

   (a) Calculate the upper limit of the input common-mode voltage range.

   (b) Calculate the upper limit of the output voltage range when the input common-mode voltage is 0.2 V

   (c) Calculate all transistor widths for a slew rate equal to 200 V/μs.