LAYOUT TUTORIAL

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Objectives

1. Draw the schematic diagram in Figure 1.
2. Create the NMOS and PMOS layout
3. Create the P type resistor layout
4. Pass design rule check (DRC)
5. Pass layout versus schematic (LVS)
6. Create a symbol for the layout diagram
7. Simulate layout using Cadence

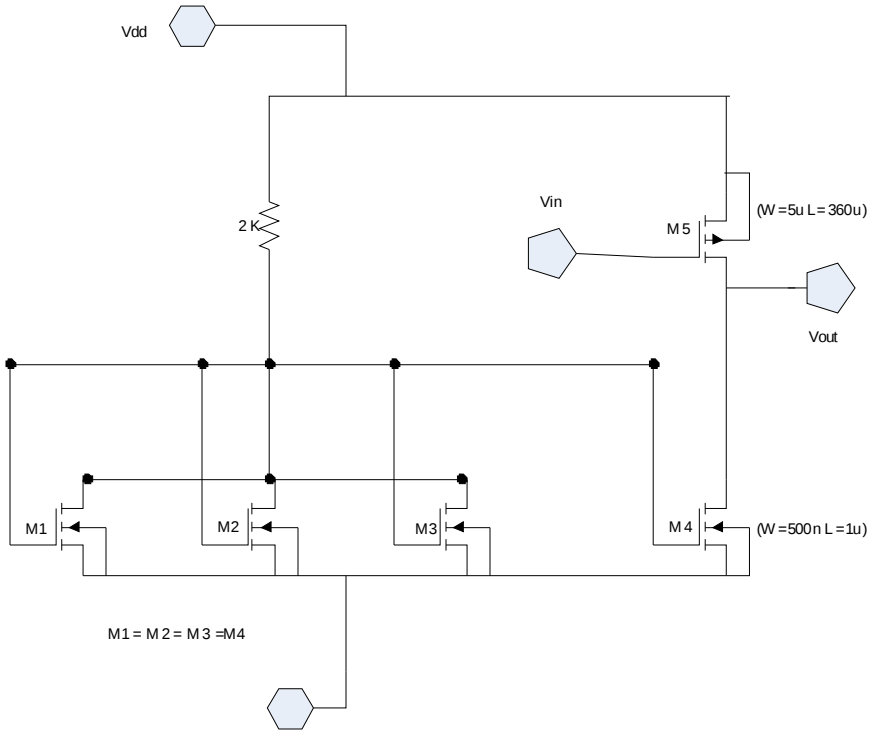

Fig 1. Schematic Diagram

Procedure

1. Create Layout Cellview
2. Optimize the display grid
3. Create NMOS transistor and do DRC check
4. Create PMOS transistor and do DRC check
5. Create a P type Resistor and do DRC check
6. Obtain the final layout and do DRC check
7. Extract the final layout and do LVS check
8. Create a symbol for your layout
9. Simulate your layout using Cadence

Before you start creating your layout cellview, you may want to finish drawing the schematic diagram shown in Fig 1. or you can finish drawing once you have your layout diagram completed.

1. Create Layout Cellview

1. From the Library manager, choose **File** => **New** => **Cellview**
2. Enter Library Name (User define) and Cell Name NMOS
3. Choose **Virtuoso** as the design tool
4. Click OK and the design window will pop-up

Note: Use the **F4** function key on your keyboard can switch the mode to Partial mode. This will allow you to select the entire object, a part, an edge or a corner of it

The **Layer Selection Window** (**LSW**) will let you select different layers of the mask layout. The LSW can be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the LSW.

Virtuoso is the main layout editor of Cadence design tools.

2. Optimize the display gird

Before you start drawing your first transistor, you will set up the display space first. We will set the minor grid dots to display every 0.01 microns, and the major ones to display every 0.05 microns.

1. Select **Options** => **Display**
2. Set the **Minor Spacing** to 0.01
3. Set the **Major Spacing** to 0.05
4. Set **X Snap Spacing** to 0.01
5. Set **Y Snap Spacing** to 0.01
6. Select **Options** => **Layout Editor…**=> **Aperture** to 0.01 (This is set up your mouse step value)
7. Choose **Window** => **Redraw** on the Virtuoso Editor window to redraw your layer

3. Create NMOS transistor

Once you have set the proper display grid, you can start drawing the NMOS transistor. The NMOS transistor consists of the N-Diffusion layer, the gate poly, and the active contacts and a p-substrate. The active contact is composed of **metal1** make and a contact cut, which connects the metal1 above to the source/drain diffusion areas. The complete NMOS transistor layout can be seen in Fig 2.

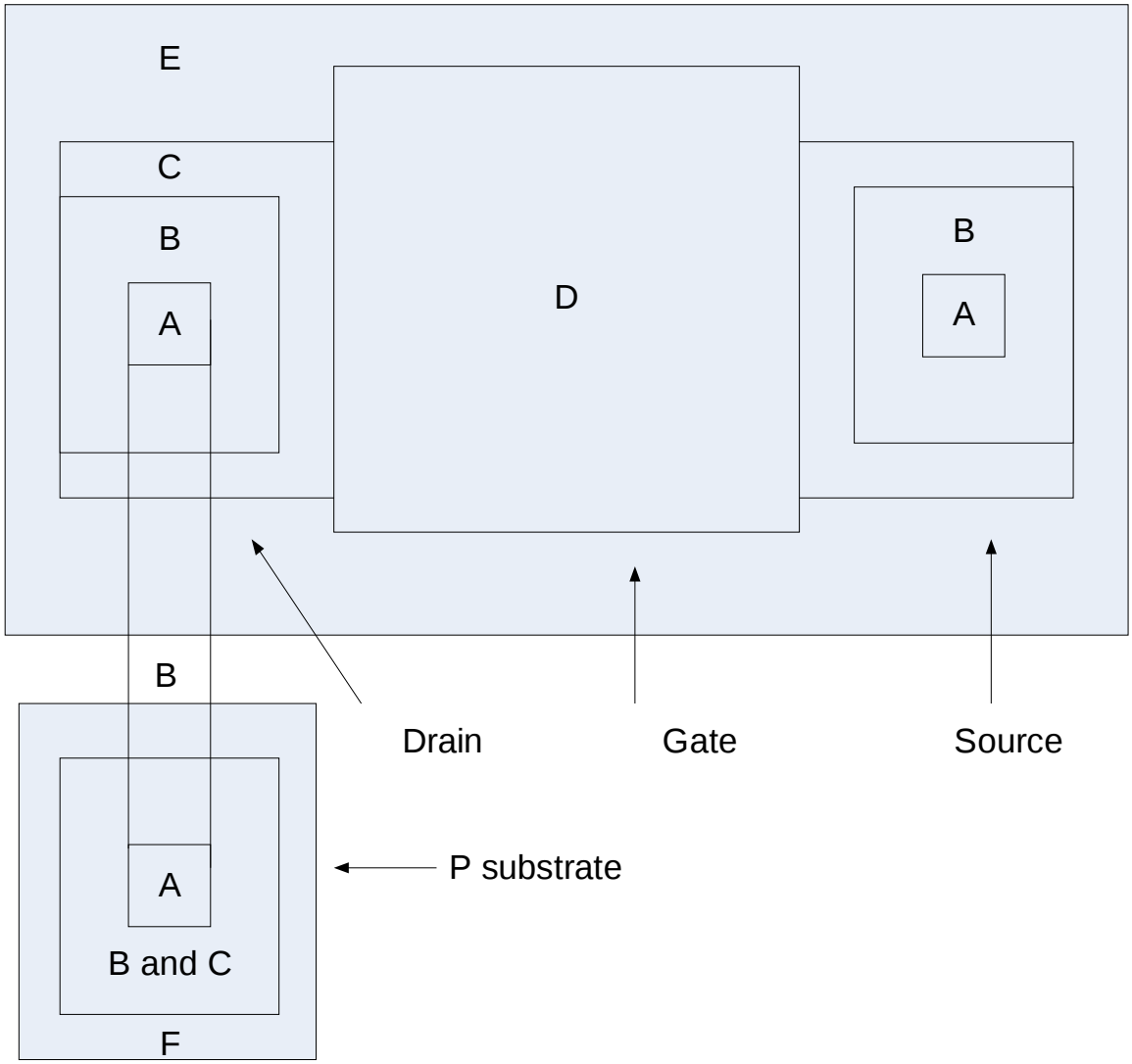

Fig 2. NMOS transistor Layout

A is contact (dg), B is Metal1(dg), C is Active (dg), D is poly1(dg), E is nplus, F is pplus

To set up the exact dimension more easily, you can use the ruler. Click on the **Ruler icon** from the left window, or select **Window => Create Ruler**. To erase the ruler, simply by choosing **Window => Clear All Rulers.** Now we can work on the NMOS transistor.

1. Select **nplus dg** layer from the LSW and draw a rectangle a rectangle with $X = 2.48\mu m$ and $Y = 1.36\mu m$ (suggested size only)
2. Select **active dg** layer from the LSW and draw a rectangle with $X = 2.12\mu m$ and $Y = 0.5\mu m$ (suggested size only)
3. Select **poly dg** layer from the LSW. Select **path icon** from the left screen and enter $Width = 1$ which indicates the length of your poly. Draw a $1\mu m$ long path this indicates the width of your transistor. (X value is fixed and Y value is at least)
4. Select **contact dg** layer and draw a square with $X = Y = 0.22\mu m$ (suggested size only)
5. Select **metal1 dg** layer and draw a square with $X = Y = 0.46\mu m$ (suggested size only)

6. Draw a square using **pplus dg** layer with $X = Y = 0.62\mu m$ (suggested size only)
7. Copy the square created from step 5 by selecting the square and use **C** key on your keyboard
8. Copy the square created from step 7 and chance its property to **Active dg.** To change the property, click the right mouse and select **Active dg** and OK
9. Copy the contact create from step 4
10. To create a p-substrate, gather **pplus dg** square, **metal1 dg** square, **active dg** square, and **contact dg** square shown in Fig 2
11. Choose path (**metal1 dg**) to connect p substrate with drain
12. Select **Verify** => **DRC** => **OK** and you should see errors
13. Select **Verify** => **Markers** => **explain**.

You will see the following message

reason: floating poly1
reason: Warning : substrate/well soft connected add power/ground label if necessary

14. Select **Verity** => **Markers**=>**Delete All** to clear the markers if you have no other errors besides those two.

4. Create PMOS Transistor

Now we can start drawing the PMOS transistor. The PMOS transistor consists of the P-Diffusion layer, the gate poly, the active contacts, an nwell and a n-substrate. The complete PMOS transistor layout can be seen in Fig 3.

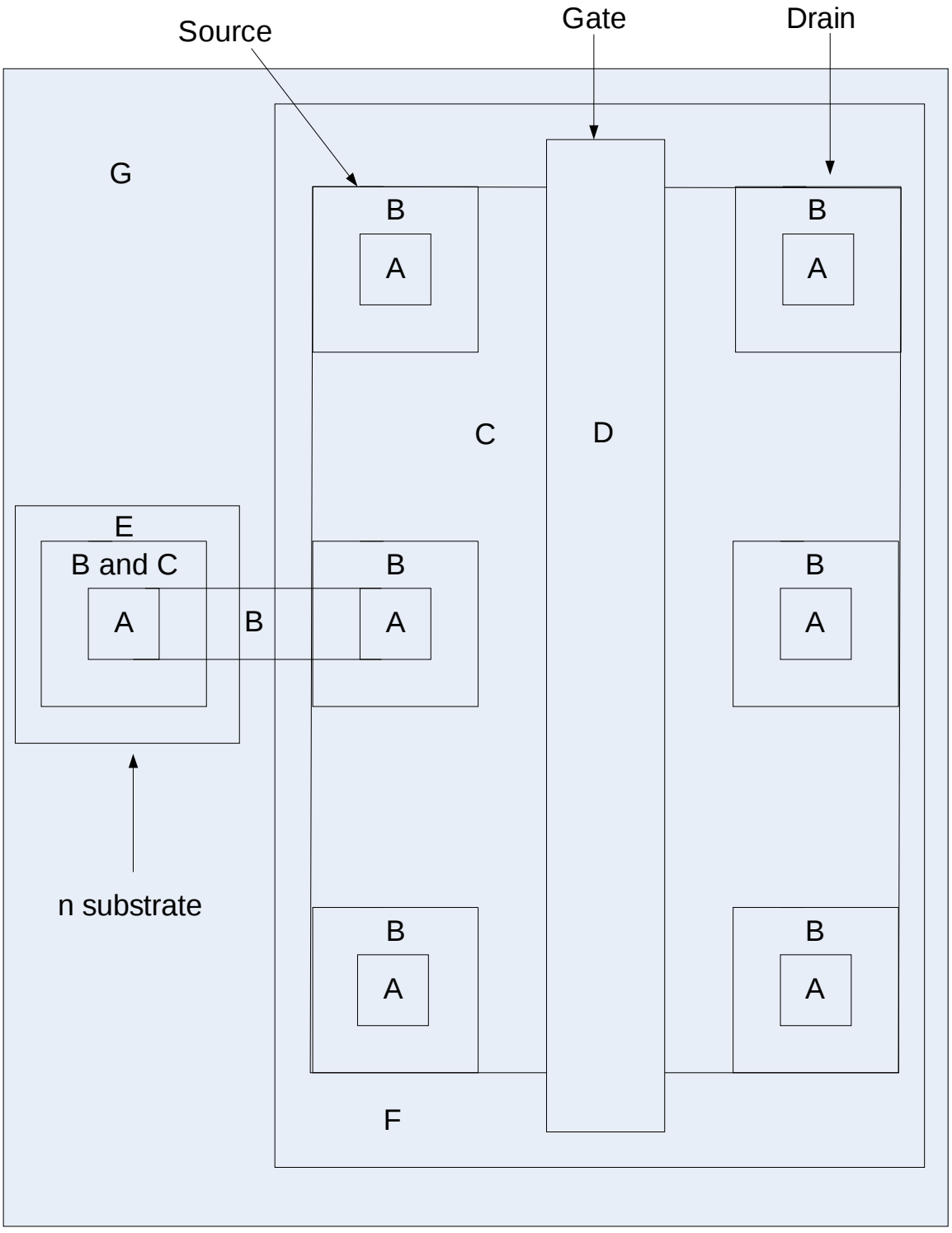

Fig 3. PMOS transistor layout

A is contact (dg), B is Metal1(dg), C is Active (dg), D is poly1(dg), E is nplus, F is pplus.
G is nwell

1. Select **nwell dg** layer from the LSW and draw a rectangle with $X = 2.4\mu m$ and $Y = 5.9\mu m$ (suggested size only)

2. Select **pplus dg** layer from the LSW and draw a rectangle with $X = 1.84\mu m$ and $Y = 5.7\mu m$ (suggested size only)
3. Select **active dg** layer from the LSW and draw a rectangle with $X = 1.48\mu m$ and $Y = 5\mu m$ (suggested size only)
4. Select **poly dg** layer from the LSW. Draw a path with $X = 0.36\mu m$ and $Y = 5.5\mu m$ (X value is fixed and Y value is at least)
5. Select **contact dg** layer and draw a square with $X = Y = 0.22\mu m$ (suggested size only)
6. Select **metal1 dg** layer and draw a square with $X = Y = 0.46\mu m$ (suggested size only)
7. Draw a square using **nplus dg** layer with $X = Y = 0.62\mu m$ (suggested size only)
8. Copy the square created from step 6 by selecting the square
9. Copy the square created from step 8 and change its property to **Active dg.**
10. To create a n-substrate, gather **nplus dg** square, **active dg** square, **metal1dg** square, **contact dg** square as shown in **Fig 3.**
11. Connect n-substrate to the source of NMOS transistor
12. Select **Verify** => **DRC** => **OK** and you should see errors
13. Select **Verify** => **Markers** => **explain**.

You will see the following message

reason: floating poly1
reason: Warning : substrate/well soft connected add power/ground label if necessary

15. Select **Verity** => **Markers**=>**Delete All** to clear the markers if you have no other errors besides those three.

5. Create P type Resistor

Once you have create the NMOS and PMOS transistor, you can start drawing a p type resistor. This type of resistor is used to connect between the power source and other components. Another type of resistor is call n type resistor which is used to connect the components and ground. We will only discuss p type resistor here. The layout of a p type resistor is shown in **Fig 4**.

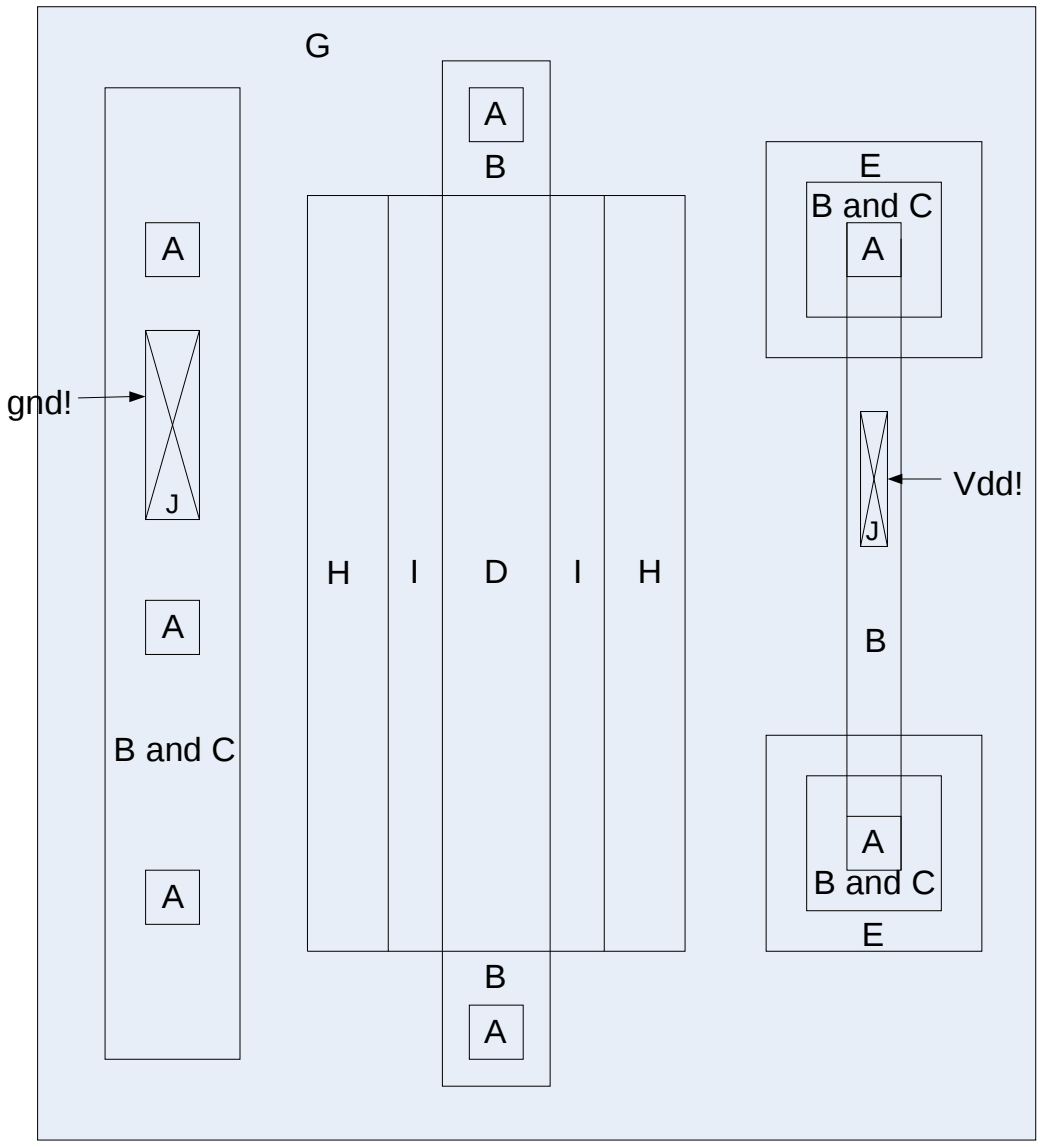

Fig 4. P type Resistor layout

A is contact (dg), B is Metal1 (dg), C is Active (dg), D is poly1 (dg), E is nplus (dg), F is pplus (dg), G is nwell (dg), H is rop (dg), I is plres (dg), J is Metal1 (pn)

1. Select **rpo dg** layer and draw a rectangle with $X = 0.86\mu m$ and $Y = 2.7\mu m$
2. Select **plres dg** layer and draw a rectangle with $X = 0.62\mu m$ and $Y = 2.7\mu m$
3. Select **poly1 dg** layer and draw a rectangle with $X = 0.42\mu m$ and $Y = 4\mu m$

Note: The area covered by **plres dg** layer defines the resistor value.

The next step is to create a vdd! pin and a gnd! pin and this will allow us to pass the DRC without any errors.

4. Select **metal1 pn** layer and select **Create** => **Pin** => **shape pin**. Type in vdd! and gnd! in the **Terminal Names** box and choose **inputOutput** at the I/O Type.
5. Complete the rest of the layout shown in Fig 4.
6. Select **Verify => DRC => OK.** You should see no errors.
7. Select **Verify => Extract=> OK**
8. Open the extracted file from your library manger window
9. Click shift + f to see the resistor value and click ctrl + f to change the mode

The resistor value should be 1999.29 Kohm shown in the extracted file.

6. Obtain the final layout and do DRC check

Open a new Cellview under the library you created above. Insert 4 NMOS transistors, 1 PMOS transistor, and 1 2Kohm resistor. Build the circuit using those components as shown in Fig 1.

To create a power source, use **Metal1 dg** to draw a big rectangle and name it vdd! using **Metal1 (pn)**. Create another rectangle with **Metal1 dg** and name it gnd! using **Metal1 (pn)**.

Don't forget to label your input and output using **Metal1 (pn)** as well. Once you have your layout diagram wired, do DRC. If there are no errors, procees to the next section

7. Extract the final layout and do LVS check

1. **Verify => Extract =>OK**.
2. Open your extracted layout view from the Library Manger and select **Verify => LVS => Run**. To check if there are any errors, click on **Error Display** in the LVS window. There should be no errors. Click on **Output** in the LVS window, you will see your output results between your layout and schematic and they should match.

8. Create a symbol for your Layout

1. Open your schematic diagram
2. Select **Design => Create Cellview => From Cellview => OK => OK**
3. Select **Add => Pin**
4. Enter vdd! gnd! in the **Pin Names** box and select **inputOutput** under Direction option
5. The symbol is shown in **Fig 5**.

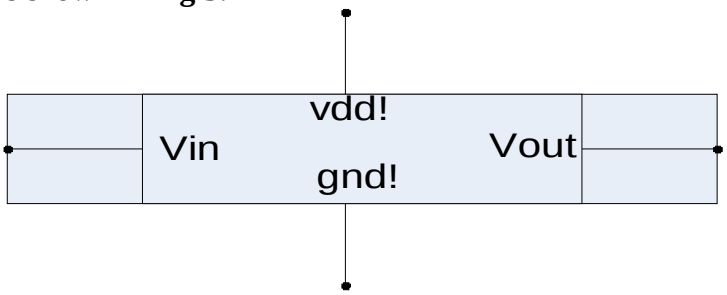

Fig 5. Symbol view create from the schematic

9. Simulate your layout using Cadence

1. Create a new schematic diagram
2. Select **Add => Instance** and Browse the symbol you just created
3. Select **Add => Instance =>analogLib => vdd => symbol**
4. Select **Add => Instance =>analogLib => vdc => symbol**
5. Select **Add => Instance =>analogLib => gnd => symbol**
6. Select **Add =. Pin** => Enter Vout in the **Pin Names** box => Change Direction to output in the **Direction** option
7. Draw the schematic diagram as shown in Fig 6.

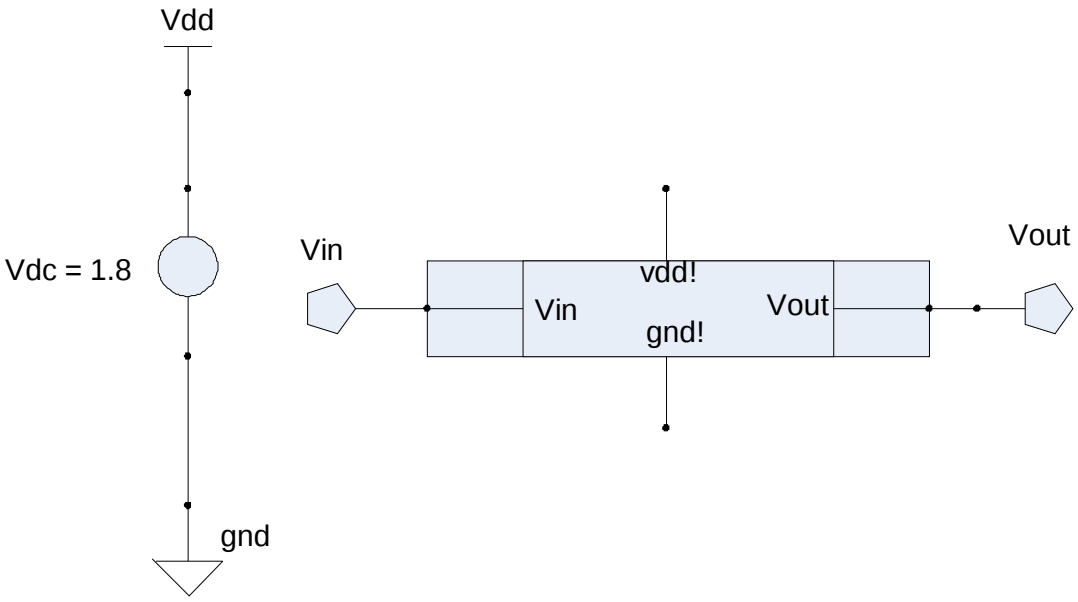

Fig 6. Final Schematic Diagram

8. Select **Tool => Analog Environment => Setup => Simulator/Directory/Host => spectreS => OK**
9. Select **Setup => Environment**
10. Enter a word **extracted** in front of the schematic in the **Switch View List** box
11. Use **spectre** instead of cdsSpice =**OK**

You can work on different type of analysis with different type of input. This is the end of the tutorial.