

EELE0531: Analog CMOS Integrated Circuits Run Cadence

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2019

1 Prepare For Schematic

Before read this document, please refer to the Log-in-steps, posted on the course website. You **MUST** have successfully log-in to the server to start the following step.

To start Cadence, there are a few steps that you need to complete. Once you have successfully log-in, you will be led to the home directory as */home-/user*. A good starting point will be creating a design folder, i.e. type *mkdir design*. A new folder, *"design"*, is created. You are strongly recommended to have a Linux/Unix reference by hand. In particular, some most often used commands, e.g. *cd*, *list*, *echo*, *etc.*, should be familiarized. Now type *cd design*. Then type */CMC/bin/goCadence*. A new window pops-up. Scroll down to the bottom. Choose 180 nm as shown in Fig. 1 a). **icfb** interface

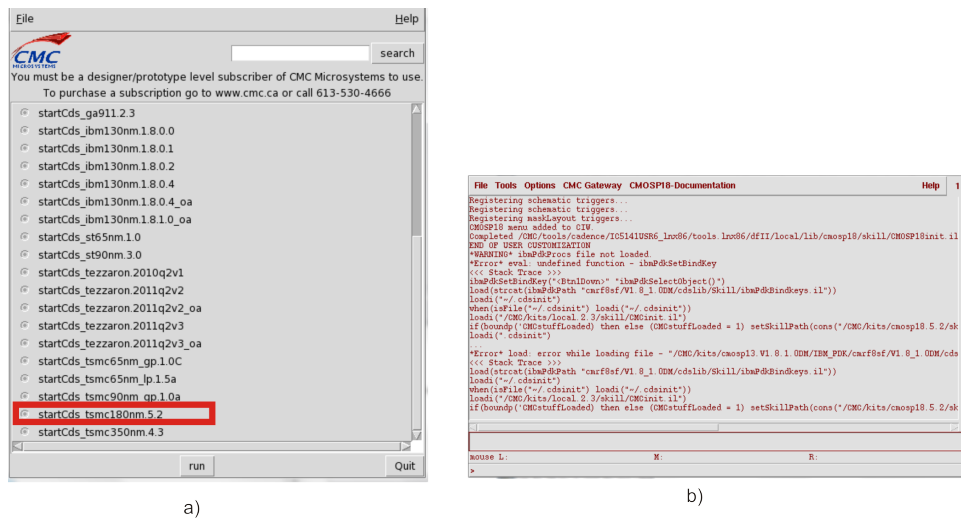


Figure 1: a) Start window b) icfb

in Fig. 1 b) is the design framework (DFII) front-end for the CIC platform. From **icfb** you will be able to access all the tools for schematic capture, symbol editing, simulation, layout, DRC and LVS checking, and extraction.

Next step is to create a working library, which **must** be attached to the 180 nm technology so as to create the link between the design library and the

technology library. To do that, go to **icfb->File->New->Library**. Name the library **lab1**, and under Technology File choose **Attach to an existing techfile** and press OK. In the popup window, choose cmosp18 from the drop-down list beside Technology Library.

To create a schematic cellview, go to **icfb->File>New->Cellview**. Change the Library Name to **lab1**, and make the Cell Name **nmos(for example)**. Leave the View Name and Tool as is. An empty Virtuoso Schematic Editor Fig. 2 window will open.

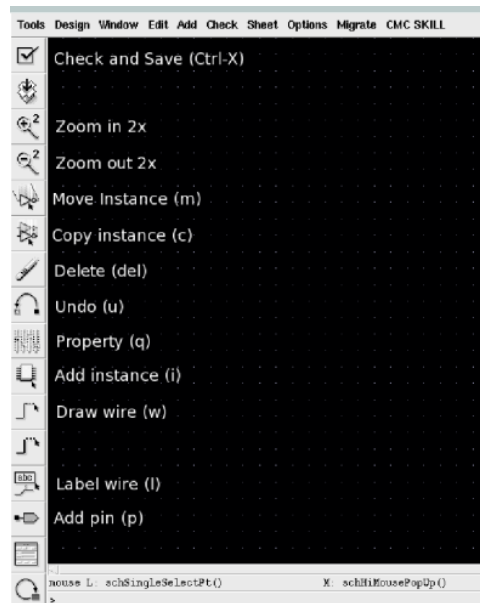


Figure 2: Schematic editor

If you are in this step, you should not have issues with Cadence account. Please refer to the EELE0531 Lab Manual.