PELGROM'S MODEL OF MISMATCH (§ 4.6.1) ①

- V_{th} MISMATCH FOR ONE TRANSISTOR IS APPROXIMATED AS FOLLOWS: (NOTE CONTRADICTION IN § 4.6.1 AND § 5.1.4)

$$\sigma(\Delta V_{th}) \simeq \frac{A_{VT}}{\sqrt{WL}}$$

A_{VT}: MISMATCH THRESHOLD COEFFICIENT $[mV\,\mu m]$

PRACTICALLY, A_{VT} CAN BE ESTIMATED AS:

$$A_{VT}(mV\,\mu m) \simeq t_{ox}(nm)$$

EXAMPLE

$t_{ox} = 41\,\text{Å}$ FOR A 180 nm PROCESS, SUPPOSE $W = L = 1\,\mu m$

$41\,\text{Å} = 4.1\,nm$

$$\sigma(\Delta V_{th}) = 4.1\,mV$$ STANDARD DEVIATION.

- DIFFERENCES IN SPECIFIC CURRENT ARE ALSO ESTIMATED AS A FUNCTION OF $\sqrt{WL}$:

$$\sigma\left(\frac{\Delta I_{SQ}}{I_{SQ}}\right) = \frac{A_\beta}{\sqrt{WL}} = \sigma\left(\frac{\Delta\beta}{\beta}\right);\ \beta = \mu C_{ox}\frac{W}{L}$$

$A_\beta \simeq 1\%\,\mu m - 3\%\,\mu m$ (USE 3% FOR WORST-CASE)

EXAMPLE: $W = L = 1\,\mu m \Rightarrow \frac{\Delta I_{SQ}}{I_{SQ}} \simeq 3\%$

VALID ONLY IF TRANSISTORS NOT VERY LONG/NARROW

APPLICATION TO CURRENT MIRRORS

$$\left|\frac{\Delta I_D}{I_D}\right| \simeq \therefore \left|\frac{\partial I_D}{\partial V_{th}}\right|\frac{\Delta V_{th}}{I_D} + \left|\frac{\partial I_D}{\partial I_S}\right|\frac{\Delta I_S}{I_D}$$

(SINCE SIGN OF ΔV_{th}, ΔI_S UNKNOWN)

$$\left|\frac{\partial I_D}{\partial V_{th}}\right| = \left|\frac{\partial I_D}{\partial V_G}\right| = g_{mg} = \frac{2I_S}{nV_T}\left(\sqrt{1+i_f}-1\right) \quad \text{(FOR ACTIVE)}$$

$$\left|\frac{\partial I_D}{\partial I_S}\right| = i_f$$

$$\left|\frac{\Delta I_D}{I_D}\right| \simeq \frac{g_m}{I_D}\Delta V_{th} + \frac{i_f}{I_S i_f}\Delta I_S$$

ADDED TO ACCOUNT VARIATIONS IN 2 TRANS.

$$\frac{g_m}{I_D} = \frac{2}{nV_T}\frac{\sqrt{1+i_f}-1}{i_f} = \frac{2}{nV_T\left(\sqrt{1+i_f}+1\right)}$$

$$\therefore \sigma\left(\frac{\Delta I_D}{I_D}\right)^2 \simeq \left[\underbrace{\left(\frac{2}{nV_T}\frac{1}{\sqrt{1+i_f}+1}\frac{A_{VT}}{\sqrt{WL}}\right)^2}_{\sigma(\Delta V_{th})^2} + \underbrace{\left(\frac{A_\beta}{\sqrt{WL}}\right)^2}_{\sigma\left(\frac{\Delta I_S}{I_S}\right)^2}\right] \times 2$$

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 \simeq \left[\left(\frac{2A_{VT}}{nV_T\left(\sqrt{1+i_f}+1\right)}\right)^2 + A_\beta^2\right]\frac{2}{WL}$$

- HOWEVER, A MORE ACCURATE EXPRESSION IS

$$\boxed{\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 = \frac{2}{WL}\left[\left(\frac{A_{VT}}{nV_T}\right)^2\frac{\ln(1+i_f)}{i_f} + A_\beta^2\right]}$$

BETTER FOR $i_f > 1$, AND SAME FOR $i_f < 1$

EXAMPLE

$n = 1.2$

- FOR A GIVEN PROCESS, $A_{V_T} = 4\ \frac{mV}{\mu m}$, $A_\beta = 2\ \%/\mu m$
- CALCULATE MINIMUM GATE AREA FOR $\sigma\left(\frac{\Delta I_D}{I_D}\right) = 5\%$

IF $i_f = 0.05, 1, 100$

$$WL = \frac{2}{\sigma\left(\frac{\Delta I_D}{I_D}\right)^2}\left[\left(\frac{A_{VT}}{nV_T}\right)^2 \frac{\ln(1+i_f)}{i_f} + A_\beta^2\right]$$

$$WL = \frac{2}{2.5\times10^{-3}}\left[16.4\,\mu m^2 \underbrace{\frac{\ln(1+i_f)}{i_f}}_{\text{(a) } 0.05 \to 0.975,\ \text{(b) } 1 \to 0.69,\ \text{(c) } 100 \to 0.046} + 0.4\,\mu m^2\right]$$

$$WL = \begin{cases} 13112\ \mu m^2 \\ 9373\ \mu m^2 \\ 923\ \mu m^2 \end{cases} \longrightarrow \text{NOTE HUGE EFFECT ON REQUIRED AREA DUE TO INVERSION LEVEL.}$$

- TO DECIDE SIZE OF UNIT TRANSISTOR, USE THE MAXIMUM CHARACTERIZED MOSFET FOR A TECHNOLOGY AS A GUIDELINE. FOR EXAMPLE, IF MAXIMUM SIZE IS $\frac{100\,\mu m}{20\,\mu m}$

(c) COULD BE REALIZED WITH A SINGLE TRANSISTOR $\frac{100\,\mu m}{10\,\mu m}$ (ASSUMING THIS GIVES THE REQUIRED INVERSION LEVEL)

(b) NEEDS 10 UNIT TRANSISTORS $\left(\frac{100\,\mu m}{20\,\mu m}\right)$

(a) NEEDS $\approx$ 12 UNITS $\left(\frac{100}{20}\right)$