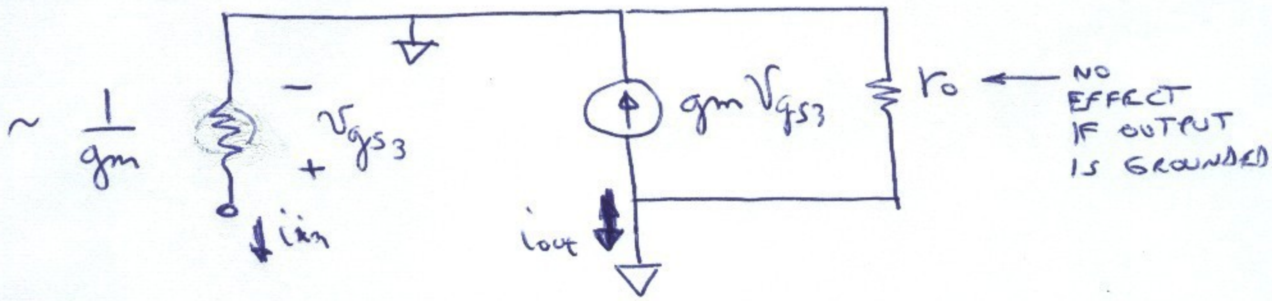
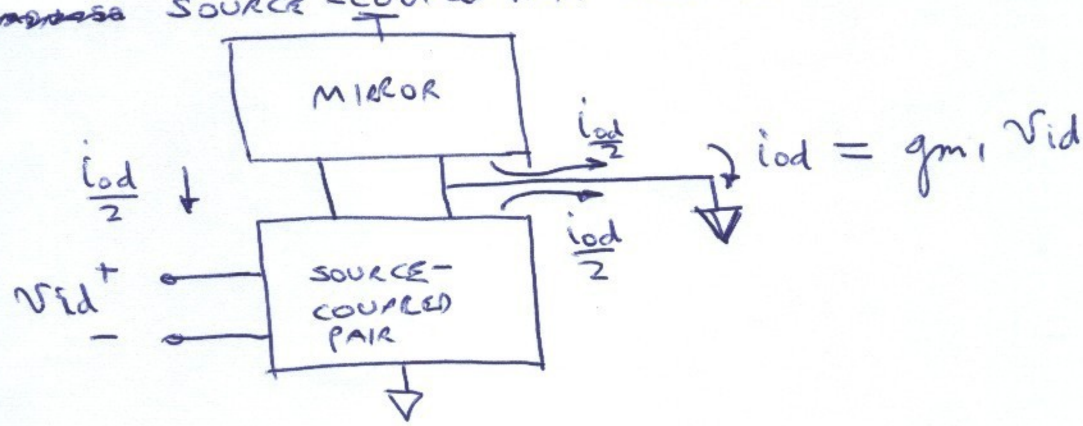
CURRENT-MIRROR LOADED DIFFERENTIAL AMPLIFIER

- CURRENT MIRROR ALONE:

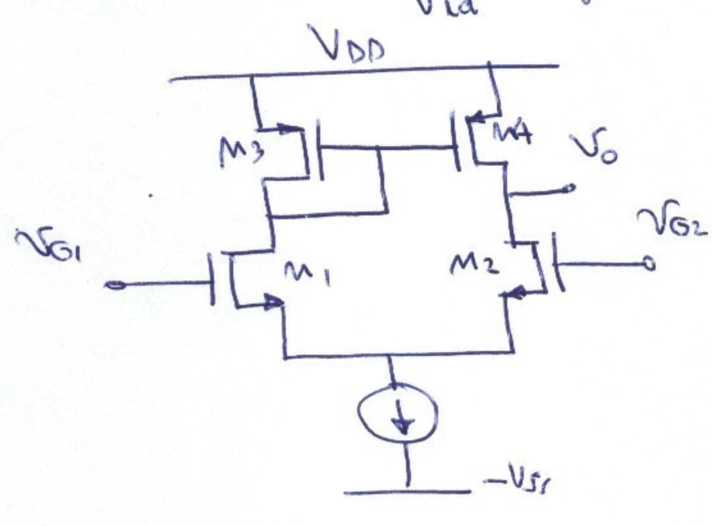


$$i_{out} = i_{in}$$

- SOURCE-COUPLED PAIR COUPLED WITH CURRENT MIRROR:



- EFFECT OF OUTPUT RESISTANCE OF TRANSISTORS:
  - OUTPUT NO LONGER GROUNDED
  - TOTAL ~~CURRENT~~ TRANSCONDUCTANCE: g_{m1}
  - TOTAL RESISTANCE: $r_{o2} \| r_{o4}$
  - VOLTAGE GAIN $= \frac{v_o}{v_{id}} = g_{m1} (r_{o2} \| r_{o4})$



$(I_{S1} = I_{S2})$

$$g_{m1} = \frac{\not{2}\, I_T}{\not{2}\, n V_T} \frac{1}{\sqrt{1+\frac{I_T}{2I_{S1}}} + 1}$$

$$r_{o2} = \frac{L_2}{I_D \left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}, \quad r_{o4} = \frac{L_4}{I_D \left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}$$

$$\frac{1}{r_{o2} \,//\, r_{o4}} = \frac{I_T}{2}\left[\frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}{L_2} + \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}{L_4}\right]$$

$$a_{dm} = \frac{v_o}{v_{id}} = \frac{\frac{\not{I_T}}{n V_T}}{\frac{\not{I_T}}{2}\left[\frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}{L_2} + \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}{L_4}\right]\left[\sqrt{1+\frac{I_T}{2I_{S}}} + 1\right]}$$

$$= \frac{2}{n V_T} \times \frac{1}{\sqrt{1+i_{f1}} + 1} \times \frac{1}{\frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}{L_2} + \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}{L_4}}$$

- a_{dm} INCREASES WITH LOWER i_{f1}
- a_{dm} INCREASES WITH L_2, L_4. ASSUMING $L_2 = L_4 = L$

$$a_{dm} \propto L$$

- MAKING $\frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}{L_2} = \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}{L_4}$ (TO DISTRIBUTE OUTPUT RESISTANCES EQUALLY → MOST BANG FOR THE BUCK)

$$\boxed{a_{dm} = \frac{L_2}{n V_T \left|\frac{\partial X_D}{\partial V_{DS}}\right|_n \left[\sqrt{1+i_{f1}} + 1\right]}}$$

WITH : $L_4 = \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_P}{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_N}$

- IF LOAD CAPACITOR ADDED:

$$GBW \simeq \frac{g_m}{C_L}$$ → SAME AS WITH ACTIVELY-LOADED CS AMPLIFIER.

VERIFY EXPRESSION →

$$= \frac{2\, I_{S1}}{n V_T C_L}\left(\sqrt{1+i_f} - 1\right)$$ → BETTER IN STRONG INVERSION

COMMON-MODE ~~INPUT RANGE~~ REJECTION RATIO (CMRR)

$$CMRR \simeq 2\, g_{m1} R_T\, g_{m4} \left(r_{o2} \parallel r_{o4} \right)$$ (NOT CONSIDERING TRANSISTOR MISSMATCH)

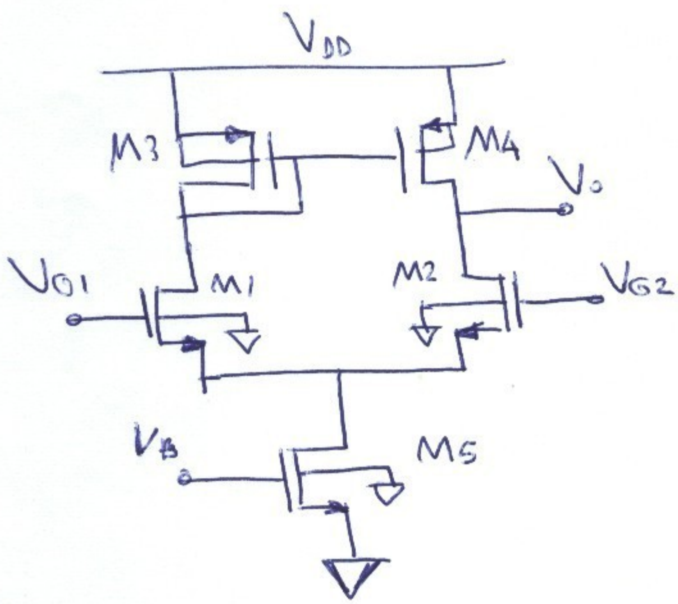
$$= 2 R_T\, g_{m4}\, a_{dm}$$

$$g_{m4} = \frac{I_T}{V_T} \frac{1}{\sqrt{1+i_{f4}}+1}$$

$$R_T = \frac{L_5}{I_T \left| \frac{\partial X_D}{\partial V_{DS}} \right|_n}$$

$$g_{m4} R_T = \frac{L_5}{V_T \left| \frac{\partial X_D}{\partial V_{DS}} \right|_n \left(\sqrt{1+i_{f4}} + 1 \right)}$$

↑ IF IMPLEMENTED WITH A SINGLE TRANSISTOR



COMMON-MODE INPUT RANGE

- SIMILAR TO CMIR OF SOURCE-COUPLED PAIR, BUT REPLACE V_D WITH $\left(V_{DD} - |V_{DS_3}| \right)$.

$$|V_{DS_3}| = |V_{GS_3}|$$

- ALSO $V_{S\,MIN} = V_{DSSAT5}$

OUTPUT VOLTAGE RANGE

$$V_{OUT\,MAX} = V_{DD} - \left| V_{DS_{SAT\,4}} \right| = V_{DD} - V_T\left(\sqrt{1+i_{f4}} + 3\right)$$

$$V_{OUT\,MIN} = \frac{V_{ICM} - V_{thn}}{n_n} - V_T\left[-5 + \ln\left(\sqrt{1+i_{f1}} - 1\right)\right]$$

OFFSET VOLTAGE

- MUST ADD TERMS DUE TO MISMATCH OF M3, M4:

$$V_{OS} \leq \Delta V_{thn} + \Delta V_{thp}\,\frac{n_n}{n_p}\,\frac{\sqrt{1+i_{f1}}+1}{\sqrt{1+i_{f4}}+1}$$

$$+\, n_n V_T\,\frac{\sqrt{1+i_{f1}}+1}{2}\left(\frac{\Delta I_{SP}}{I_{SP}} + \frac{\Delta I_{SN}}{I_{SN}}\right)$$

- FOR SIMILAR INVERSION LEVELS IN M_1, M_4 AND MODERATE OR WEAK INVERSION:

$$\boxed{V_{OS} \simeq \Delta V_{thn} + \Delta V_{thp}}$$

EXAMPLE

DESIGN A DIFFERENTIAL AMPLIFIER WITH A GAIN (DIFF) OF 2000 AND A CMRR OF 80 dB. CALCULATE THE INPUT COMMON-MODE RANGE AND THE OUTPUT VOLTAGE RANGE OF YOUR DESIGN. USE $L_{min} = 1\,\mu m$.

$n_n = n_p = 1.2$

$V_T = 26\,mV$

$V_{th_n} = -V_{th_p} = 0.4\,V$

$I_{SQn} = 100\,nA$

$I_{SQP} = 40\,nA$

$\left|\frac{\partial X_D}{\partial V_{DS}}\right|_n = 0.01\,\frac{\mu m}{V}$ $\quad \left|\frac{\partial X_D}{\partial V_{DS}}\right|_p = 0.015\,\frac{\mu m}{V}$

$$a_{dm} \cong g_{m1}\left(r_{o2} \parallel r_{o4}\right)$$

$$= \frac{\cancel{2}\, I_T}{\cancel{2}\, n V_T} \frac{1}{\sqrt{1+i_{f1}}+1} \cdot \frac{1}{\left(\frac{L_2}{\underbrace{i_{f1} I_S}_{=\frac{I_T}{2}} \left|\frac{\partial X_D}{\partial V_{DS}}\right|_n}\right)^{-1} + \left(\frac{L_4}{\underbrace{i_{f4} I_{S4}}_{=\frac{I_T}{2}} \left|\frac{\partial X_D}{\partial V_{DS}}\right|_p}\right)^{-1}}$$

$$= \frac{2}{n V_T\left(\sqrt{1+i_{f1}}+1\right)} \frac{1}{\frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_n}{L_2} + \frac{\left|\frac{\partial X_D}{\partial V_{DS}}\right|_p}{L_4}}$$

↑ MAKE THESE EQUAL

$$= \frac{L_2}{n V_T\left(\sqrt{1+i_{f1}}+1\right)\left|\frac{\partial X_D}{\partial V_{DS}}\right|_n} = 2000$$

↑ CHOOSE MODERATE–WEAK INVERSION → ~~BETTER~~ LOWER OFFSET. SHORTER L

$$\frac{L_2}{\left(\sqrt{1+i_{f1}}+1\right)} = 2000\, n V_T \left|\frac{\partial X_D}{\partial V_{DS}}\right| = 0.62\ \mu m$$

CHOOSING $i_{f1} = 10$ (MODERATE) → $L_2 = 2.67\,\mu m$

$$L_4 = \frac{0.015}{0.01} \times 2.24\,\mu m = 4.04\ \mu m$$

NOTE: IN PRACTICE YOU SHOULD LEAVE SOME MARGIN (10% OR SO)

$$CMRR \simeq 2 R_T\, g_{m4} \underbrace{a_{dm}}_{=2000} \geq 10000$$

$$\therefore R_T\, g_{m4} \geq 2.5$$ → SHOULD BE OK WITH ANY CHOICE WE MAKE.

$$I_{D4} = I_{SQp}\left(\frac{W}{L}\right)_4 i_{f4}$$

$$I_{D1} = I_{SQn}\left(\frac{W}{L}\right)_1 i_{f1}$$

→ TO EQUALIZE GATE AREAS OF NMOS AND PMOS ADJUST i_{f4}. (NORMALLY i_{f4} WOULD BE CALCULATED FROM $V_{OUT\,MAX}$.)

SINCE $I_{D4} = I_{D1}$

$$W_1 = \frac{A}{L_1} \Rightarrow \left(\frac{W}{L}\right)_1 = \frac{A}{L_1^2}, \quad \left(\frac{W}{L}\right)_4 = \frac{A}{L_4^2}$$

(A = AREA)

$$\frac{I_{sqp}}{L_4^2} i_{f4} = \frac{I_{sqn}}{L_1^2} i_{f1} \Rightarrow i_{f4} = \frac{I_{sqn}}{I_{sqp}} \frac{L_4^2}{L_1^2} i_{f1} = 56.2$$

CHOOSING $A = 10\mu m^2 \Rightarrow \begin{cases} W_1 = 4.46\ \mu m \\ W_4 \cong 2.49\ \mu m \end{cases}$

$$I_T = 2 I_{sqn} \left(\frac{3.74}{2.67}\right) \times 10 \cong 2.8\ \mu A$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{4.46\mu m}{2.24\mu m}\right)$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{3\mu m}{3.36\mu m}\right)$$

$$I_T = 2.8\ \mu A$$

$$g_{m4} = \frac{2 I_{D4}}{n V_T} \frac{1}{\sqrt{1+56.2}+1} = 0.0105\ mS$$

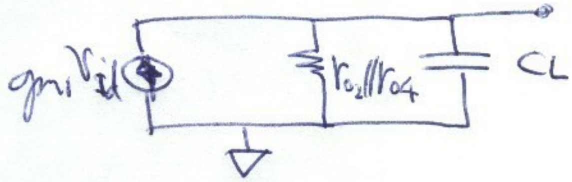
$$\therefore R_T \geq 238\ k\Omega$$

- CALCULATION OF INPUT-OUPUT RANGES LEFT AS EXERCISES..

EFFECT OF CAPACITIVE LOAD

1) FREQUENCY RESPONSE

$$v_o = g_{m1} \frac{r_{o2} \| r_{o4}}{1 + j\omega C_L (r_{o2} \| r_{o4})} \cdot v_{id}$$



$$GBW = \frac{\omega}{2\pi}\bigg|_{\left|\frac{v_o}{v_{ID}}\right| = 1} = \frac{g_{m1}}{2\pi C_L} = \frac{I_T}{n V_T C_L} \frac{1}{\sqrt{1+i_f} + 1}$$

(OK BUT DON'T USE IT!)

$$= \frac{2 I_{S1}}{n V_T C_L}\left(\sqrt{1 + i_{f1}} - 1\right)$$ ← BETTER FOR STRONG INV.

$$= \frac{2 I_{S1}}{n V_T C_L}\left(\sqrt{1 + \frac{I_T}{2 I_{S1}}} - 1\right)$$

- GIVEN GBW VALUE, 2 WAYS TO ACHIEVE IT: 1. INCREASE I_{S1}; 2. INCREASE i_{f1}
- IF i_{f1} IS BOUNDED DUE TO a_{dm} OR V_{os} CONSTRAINTS, WE CAN INCREASE $\left(\frac{W}{L}\right)_1$ $\Rightarrow I_{S1}$ TO INCREASE GBW.
  - ↳ TRADE OFF → MORE AREA; MORE TAIL CURRENT
- ALSO NOTE PARASITIC DRAIN CAPACITANCE INCREASES WITH W_1

2) SLEW RATE

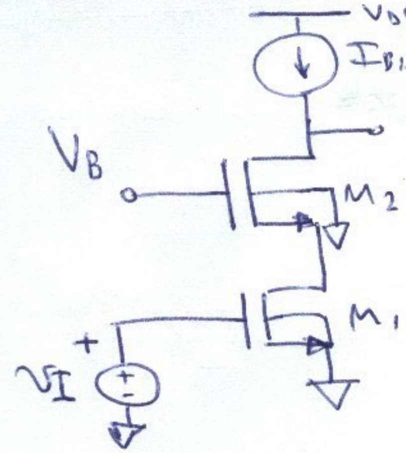
- LOAD CAPACITOR CAN BE CHARGED/DISCHARGED WITH I_T AT MOST.
- SLOPE IS: $$i_C = C_L \frac{dV_o}{dt} \Rightarrow \frac{dV_o}{dt}\bigg|_{MAX} = \frac{I_T}{C_L} \quad \text{SLEW RATE}$$

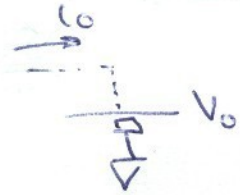
  $i_{C,MAX} = I_T$

∴ **OVERALL CONCLUSION**: A FAST AMPLIFIER REQUIRES MORE $I_T \Rightarrow$ MORE POWER CONSUMPTION.

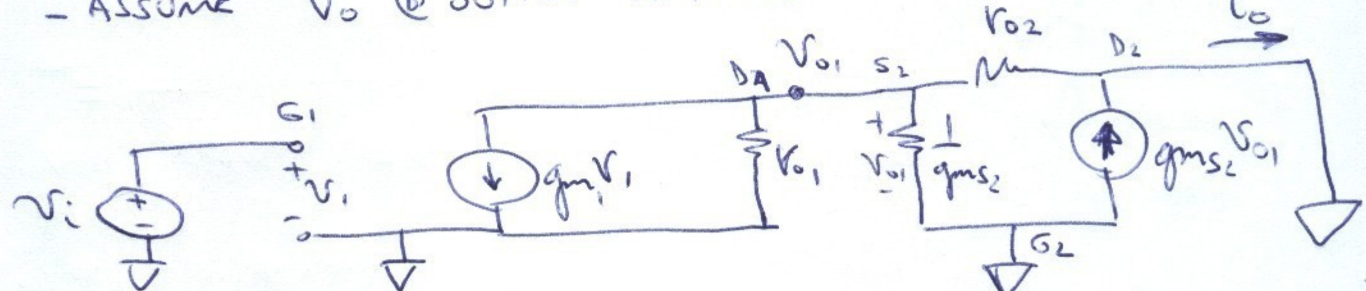
COMMON GATE - CASCODE → PAGE 16

CASCODE AMPLIFIER





- APPROXIMATE ANALYSIS USING SHORT-CIRCUIT TRANSCONDUCTANCE AND OUTPUT RESISTANCE:
  - ASSUME V_o @ OUTPUT IS FIXED



$$v_{o1} = -g_{m1} v_i \left(r_{o1} // r_{o2} // \frac{1}{g_{ms2}} \right) \approx -\frac{g_{m1}}{g_{ms2}} v_i \quad \left(\frac{1}{g_{ms2}} \ll r_{o1}, r_{o2} \right)$$

$$i_o = g_{ms2} v_{o1} + \frac{v_{o1}}{r_{o2}} \approx g_{ms2} v_{o1} \quad \left(g_{ms2} \gg \frac{1}{r_{o2}} \right)$$

∴ TOTAL TRANSCONDUCTANCE

$$\boxed{\frac{i_o}{v_i} \cong -g_{m1}}$$

SAME AS TRANSCONDUCTANCE OF C.S. AMPLIFIER

- NOW IF V_o IS LEFT FLOATING,

$$v_o = i_o \left(R_{OUT_{CASCODE}} // R_{OUT_{IBIAS}} \right)$$

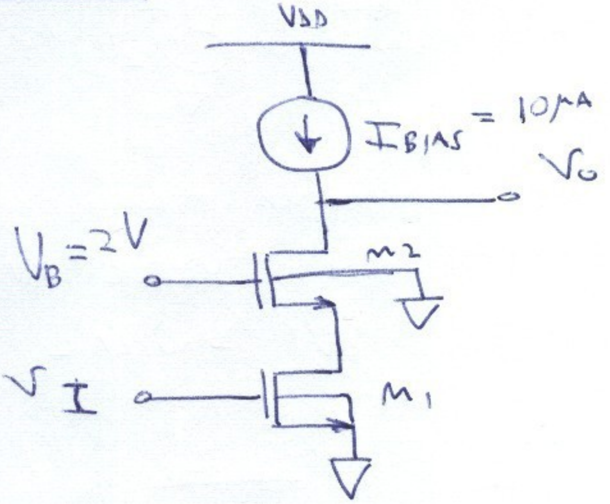
$$R_{OUT_{CASCODE}} \simeq (g_{ms2} r_{o2}) r_{o1}$$

$$\therefore \quad \frac{v_o}{v_i} \simeq -g_{m1}\left[(g_{ms} r_{o2} r_{o1}) \,//\, R_{OUT_{IBIAS}} \right]$$

$(g_{ms} r_{o2} r_{o1})$: VERY LARGE

$R_{OUT_{IBIAS}}$: IF I_{BIAS} IS ALSO CASCODED, VERY LARGE TOO

EXAMPLE



$\frac{v_o}{v_i} = ?$ $\quad V_I = ?$ $\quad V_{DS_1} = ?$

$n = 1.25$

$V_{th} = 0.6V$

$I_{S_{1,2}} = 1\mu A \qquad V_{A_1} = V_{A_2} = 25V$

$R_{OUT_{IBIAS}} = 40\, M\Omega$

a) BIASING

$$i_{f_1} = i_{f_2} = \frac{10\mu A}{1\mu A} = 10$$

$$\frac{V_I - V_{th}}{n V_T} = \mathcal{F}(10) = 2.16 \Rightarrow \boxed{V_I = 0.67V}$$

$$\frac{\frac{V_B - V_{th}}{n} - V_{S2}}{V_t} = \mathcal{F}(10) = 2.16$$

$$V_{S2} = 1.06V \Rightarrow \boxed{V_{GS_2} = 0.936V} \quad \text{(BODY EFFECT)}$$

$$g_{m1} = \frac{2 I_D}{n V_T} \frac{1}{\sqrt{1+i_f}+1} = 0.143\, mS$$

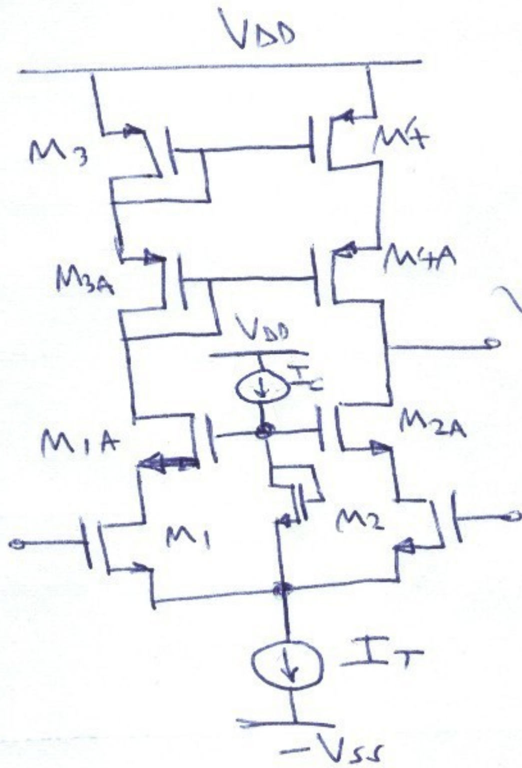
$$r_{o1} = r_{o2} = \frac{V_A}{I_D} = 2.5 M\Omega$$

$$g_{ms} = n\, g_{m1}$$

$R_{OUT} = 1.1 G\Omega$

$$\frac{v_o}{v_i} \simeq \boxed{-5,720}$$

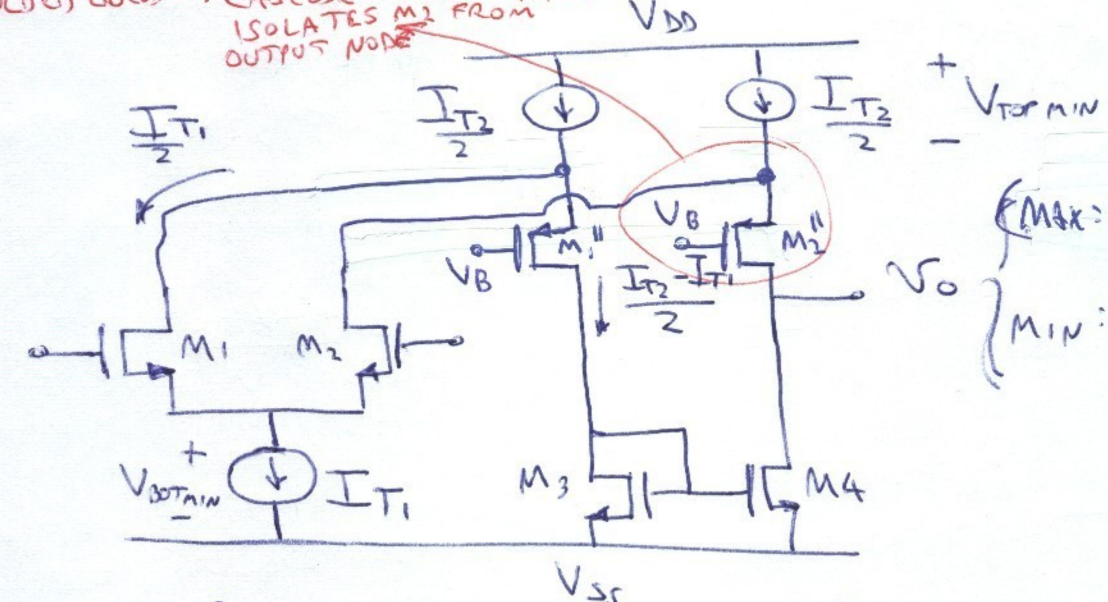
CASCODE DIFFERENTIAL AMPLIFIER



- ADVANTAGE: MORE GAIN
- DISADVANTAGE:
  - NEEDS MORE SUPPLY VOLTAGE
  - REDUCED V_O, V_{ICM} RANGE.

DIFFERENTIAL AMPLIFIER WITH IMPROVED VOLTAGE RANGE

FOLDED CASCODE: CASCODE TRANSISTOR (M_2'') ISOLATES M_2 FROM OUTPUT NODE



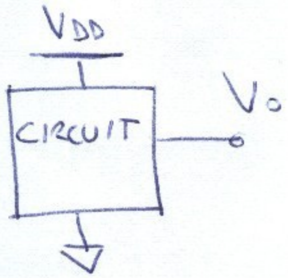
V_O MAX: $V_B + |V_{GS_{M_2''}}| - |V_{DS_{M_2'' SAT}}|$

V_O MIN: V_{DSSAT4}

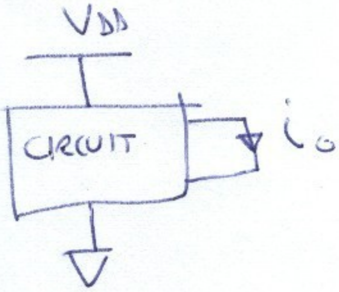
V_{ICM}:
- MAX: $V_{DD} - V_{TOPMIN} + V_{DSSAT,1} + V_{GS1}$ ← NORMALLY CLOSE OR ABOVE VDD
- MIN: $V_{BOT_{MIN}} + V_{GS1,MIN}$

- CURRENT MIRROR CAN BE CASCODED FOR EXTRA GAIN
- NEEDS EXTRA BIASING CURRENT COMPARED TO ORIGINAL.

PSRR (POWER SUPPLY REJECTION RATIO)



$$PSRR = 20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta V_o}\right)$$



$$PSRR = 20\log_{10}\left(\frac{\Delta V_{DD}}{V_{DD}}\frac{i_o}{\Delta i_o}\right)$$

EXAMPLE: