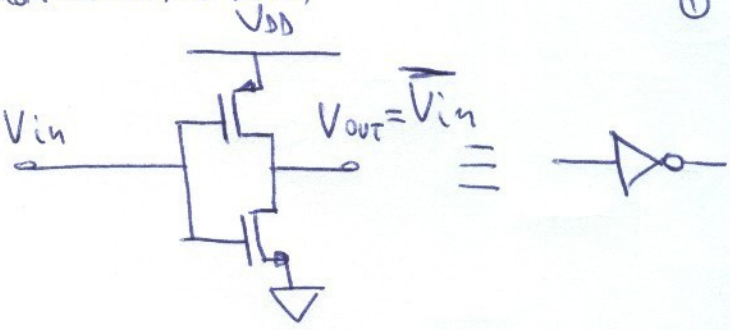
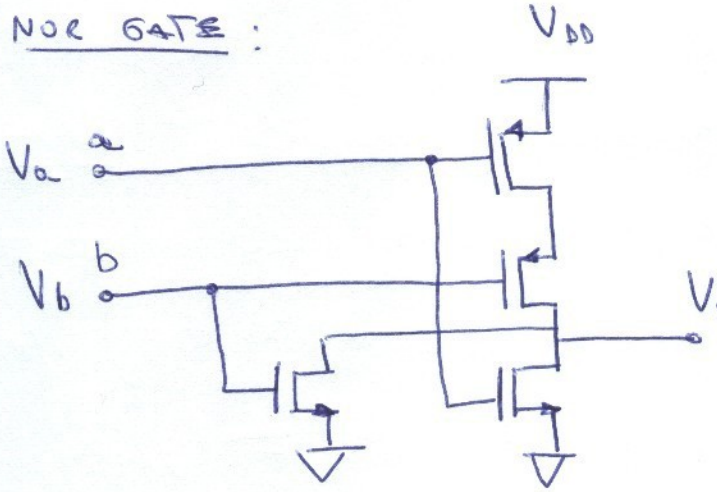
SIMPLE LOGIC GATES (FROM KEN MARTIN'S BOOK)

CMOS INVERTER :



NOR GATE :



a	b	$\overline{a+b}$
0	0	1
0	1	0
1	0	0
1	1	0

- INPUT IS CAPACITIVE
- OUTPUT NORMALLY CONNECTED TO OTHER CMOS GATES ⇒ CAPACITIVE LOAD

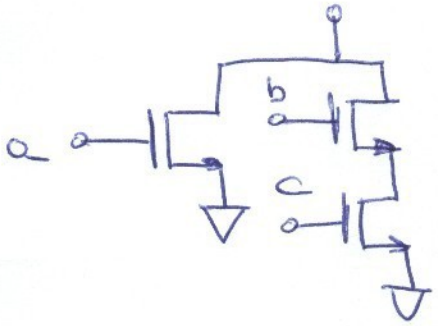
∴ NO DC CURRENTS, ONLY TRANSIENT CURRENTS TO CHARGE/DISCHARGE CAPACITORS.

- PMOS AND NMOS NETWORKS ARE COMPLEMENTARY (i.e, SWAP SERIES/PARALLEL CONNECTIONS)
- ~~$\left(\frac{W}{L}\right)$ RATIOS IN TRANSISTORS~~
- CMOS GATES WORK WITH ANY $\left(\frac{W}{L}\right)$ RATIO IN TRANSISTORS, HOWEVER, $\left(\frac{W}{L}\right)$ RATIOS HAVE AN EFFECT IN SWITCHING TIMES AND NOISE MARGIN.

EXAMPLE : DESIGN A CMOS GATE THAT PERFORMS THE FOLLOWING OPERATION : $\overline{a + bc}$

NMOS NETWORK

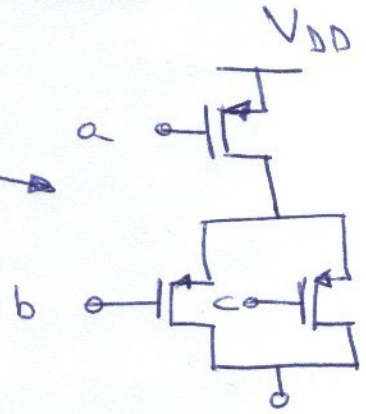
TWO BRANCHES IN //



• OUTPUT IS LOW WITH $a = 1$ OR $bc = 1$

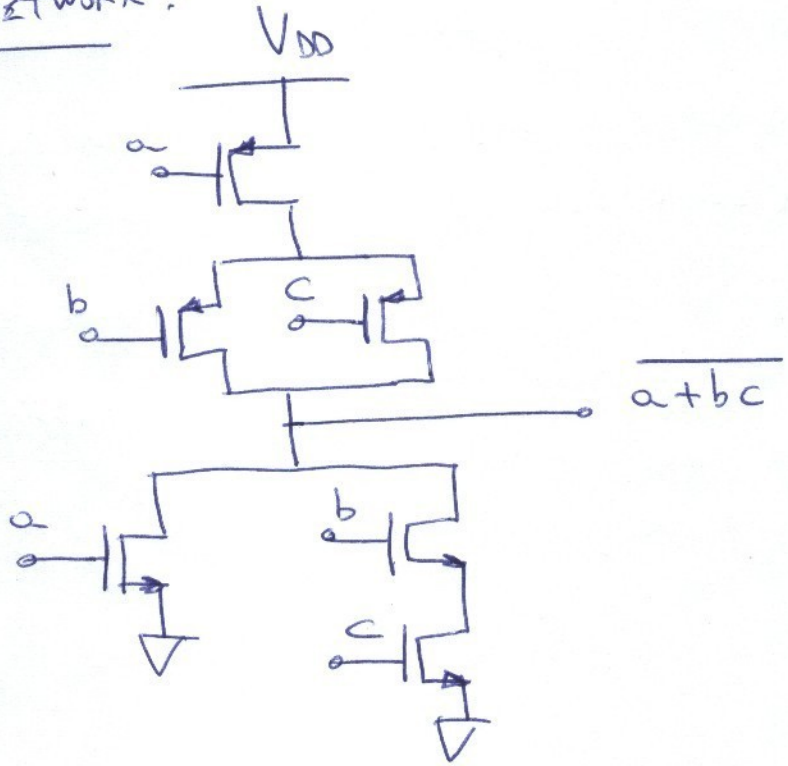
PMOS NETWORK : COMPLEMENT OF NMOS:

2 BRANCHES IN SERIES



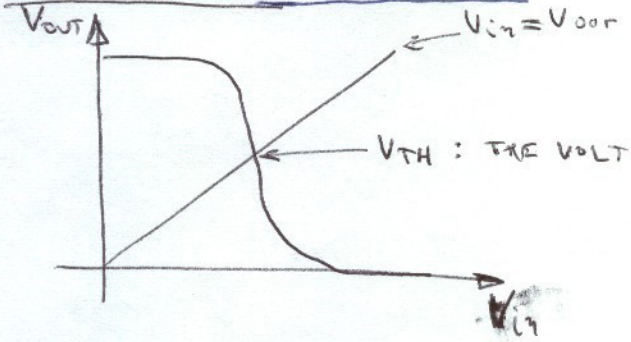
COMPLETE NETWORK :

NOTE: ROUTING GATE SIGNALS MAY BECOME COMPLICATED



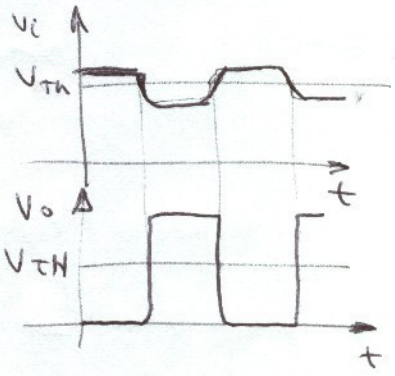
DIGITAL CIRCUIT BLOCKS

THRESHOLD VOLTAGE FOR INVERTER



- THE SMALL-SIGNAL GAIN @ V_{TH} MUST BE GREATER THAN 1 TO ENABLE A GOOD SIGNAL REGENERATION (a_v)

EXAMPLE

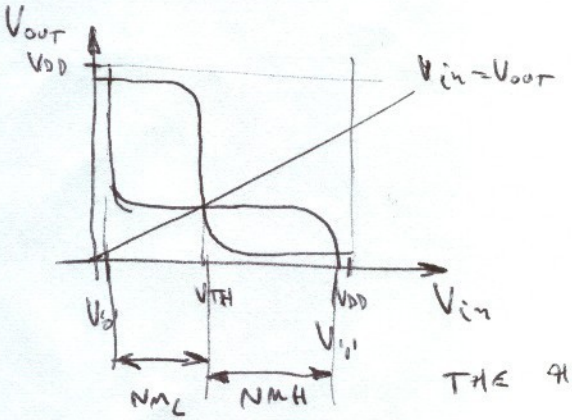


$a_v \gg 1$

TYPICALLY: $a_v = 50$ LOW-FREQ.

$a_v = 2$ FOR VERY HIGH FREQ.

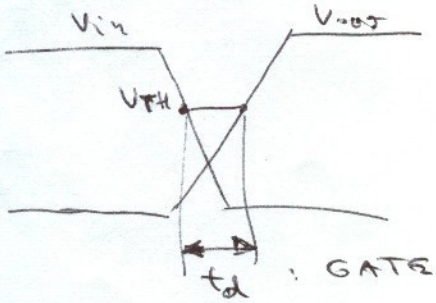
NOISE MARGIN (NM)

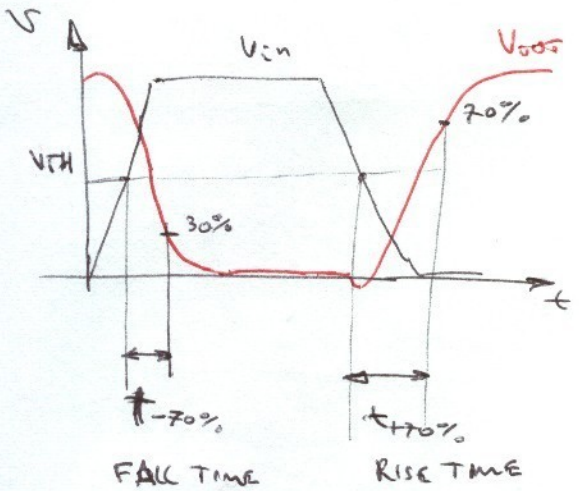


OBSERVATION: NM IS MENINGFUL ONLY IN HIGH-IMPEDANCE LOGIC FAMILIES (ie. CMOS). A BETTER PARAMETER WOULD BE A POWER NOISE MARGIN (EXAMPLE: ECL)

THE HIGHER NM → THE LESS LIKELY THE GATE HAS AN INCORRECT OUTPUT DUE TO NOISE.

GATE DELAY, RISE AND FALL TIMES

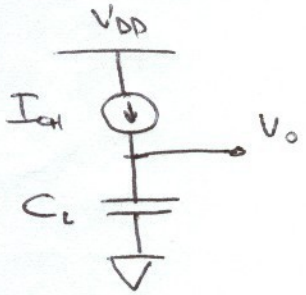




TRANSIENT RESPONSE

- EXACT ANALYSIS TOO COMPLICATED (ESSENTIALLY INTRACTABLE)
- SIMPLIFICATIONS:
  1. ALL CAPACITANCES CONNECTED TO GROUND
  2. CHARGE / DISCHARGE PRODUCED BY CURRENT SOURCES OR RESISTORS.

CASE 1:



$$\Delta V_o = \frac{I_{CH}}{C} \cdot \Delta t$$

$$I = C \frac{dV_o}{dt}$$

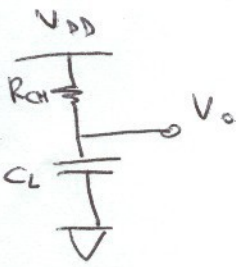
$$I = \text{CONSTANT} = I_{CH} = C \frac{\Delta V_o}{\Delta t}$$

$$\therefore \Delta t = \frac{C}{I_{CH}} \cdot \Delta V_o$$

OBSERVATIONS:

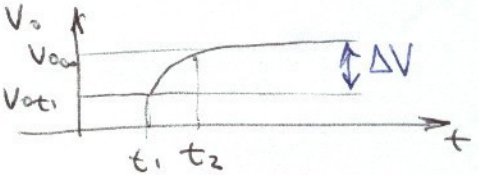
1. THE CAPACITANCE OF CRITICAL NODES MUST BE MINIMIZED
2. MINIMIZE VOLTAGE CHANGES AT CRITICAL NODES
3. MAXIMIZE CURRENTS FOR CHARGING / DISCHARGING CAPS.

CASE 2:



$$V_o(t_2) = V_{o\infty} - \underbrace{(V_{o\infty} - V_{ot1})}_{\Delta V} e^{-\frac{\Delta t}{\tau}}$$

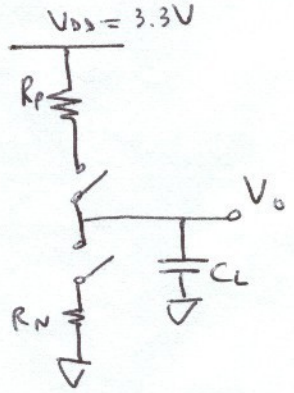
$$\tau = R_{CH} C_L$$



SOLVE FOR $\Delta t = \tau \ln\left(\frac{V_{oo} - V_{o1}}{V_{oo} - V_{o2}}\right)$

$$\boxed{\Delta t = R_{CH} C_L \ln\left(\frac{V_{DD} - V_{o1}}{V_{DD} - V_{o2}}\right)}$$

RC APPROXIMATION OF A CMOS INVERTER TRANSIENT RESPONSE



$$t_{+70\%} = R_p C_L \ln\left(\frac{3.3V - 0}{3.3V - 2.3V}\right) = 1.2 R_p C_L$$

MEASURE $t_{+70\%}$ BY SIMULATION; $C_L = 0.05pF$

$t_{+70\%} = 0.19\,ns$

$$\therefore R_p \simeq \frac{t_{+70\%}}{1.2 C_L} = 3.2\,k\Omega$$

- THAT VALUE OF R_p IS FOR A PMOS WITH $L = L_{min}$ AND $W = 5.5\mu m \Rightarrow$ R_p FOR A $1\mu m$ PMOS:

$$R_p = 3.2\,k\Omega \times 5.5\mu m = 17.6\,k\Omega\mu m$$

$$\boxed{\therefore R_p \simeq \frac{17.6\,k\Omega\,\mu m}{W}}$$

- IF C_L DOES NOT HEAVILY DEPEND ON W, THIS PROCEDURE CAN BE USED TO DETERMINE THE WIDTHS OF NMOS AND PMOS FOR GIVEN DELAY TIMES.

THRESHOLD VOLTAGE OF A CMOS INVERTER

$$I_{D1} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_1 (V_{TH} - V_{tn})^2$$

$$I_{D2} = \frac{k'_p}{2}\left(\frac{W}{L}\right)_2 \left(\underbrace{V_{DD} - V_{TH} + V_{tp}}_{|V_{ovp}|}\right)^2$$

MAKE $I_{D1} = I_{D2} \Rightarrow V_{TH} = \dfrac{V_{tn} + (V_{DD} + V_{tp})\sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_2}{\mu_n\left(\frac{W}{L}\right)_1}}}{1 + \sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_2}{\mu_n\left(\frac{W}{L}\right)_1}}}$

NOTE: $\left(\frac{W}{L}\right)_2 \uparrow \Rightarrow V_{TH} \uparrow$

EXAMPLE: $\mu_n = 575\ \frac{cm^2}{Vs}$, $\mu_p = 130\ \frac{cm^2}{Vs}$, $V_{tn} = 0.8V$, $V_{tp} = -0.9V$, $V_{DD} = 3.3V$

$\left(\frac{W}{L}\right)_1 = \frac{1.2}{0.6}$

$\left(\frac{W}{L}\right)_2 = \frac{1.8}{0.6}$

$V_{TH} = 1.4V$

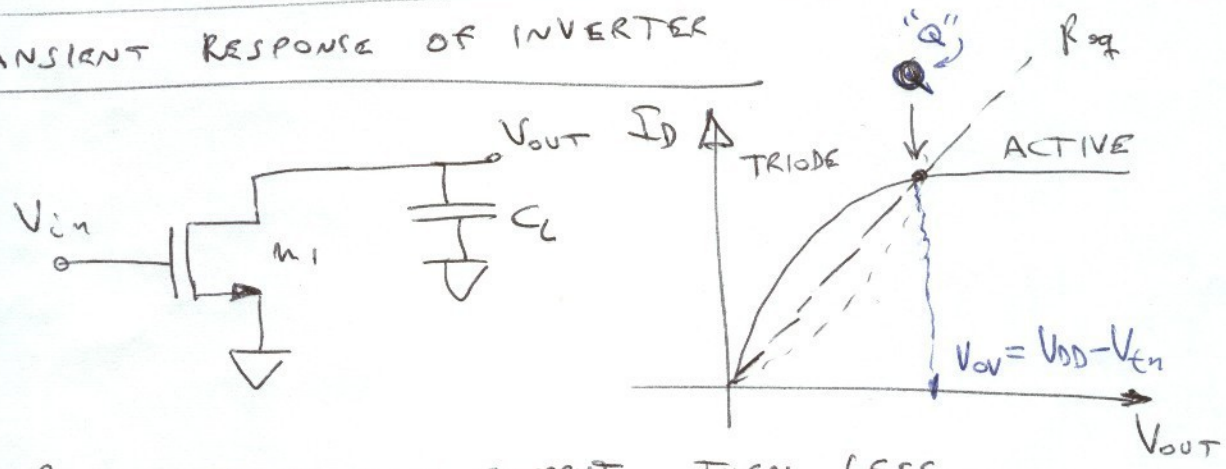
$NMH = V_{DD} - 1.4V = 1.85V$

$NML = V_{TH} = 1.4V$

IF $\left(\frac{W}{L}\right)_2 = \frac{1.2}{0.6} \rightarrow V_{TH} = 1.32V$ (LOWER)

$\left(\frac{W}{L}\right)_2 = 4\left(\frac{W}{L}\right)_1 \rightarrow V_{TH} = 1.65V$ (CLOSER TO MIDDLE)

TRANSIENT RESPONSE OF INVERTER



R_{eq} → FIRST MORE CURRENT, THEN LESS

AT 'Q', $V_{DS} = V_{DD} - V_{tn} \Rightarrow I_{D_Q} = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{tn})^2$

$$R_{eq} = \frac{V_{OUT}}{I_{DQ}} = \frac{2}{k'\left(\frac{W}{L}\right)(V_{DD} - V_{tn})}$$

• THIS UNDERESTIMATES FALL TIME → USE 2.5 INSTEAD:

$$R_{eq1} = \frac{2.5}{k_n'\left(\frac{W}{L}\right)_1 (V_{DD} - V_{tn})}$$

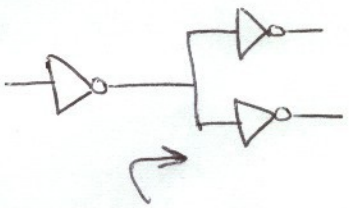
$$R_{eq2} = \frac{2.5}{k_p'\left(\frac{W}{L}\right)_2 (V_{DD} + V_{tp})}$$

$t_p \simeq R_{eq1} C_L \ln(\ )$

$t_{-70\%} \simeq 1.2\, R_{eq1} C_L$

$t_{+70\%} \simeq 1.2\, R_{eq2} C_L$

EFFECT OF TRANSISTOR SIZES ON TRANSIENT RESPONSES



$C_{gs} \simeq WLC_{ox}$ (VERY ROUGH APPROXIMATION)

NOTE: TRANSISTORS NOT ALL THE TIME IN ACTIVE REGION → GOING FROM CUTOFF TO TRIODE.

$$C_L \simeq 2C_{ox}(W_n + W_p)$$

$$t_{av} \simeq 1.2\, C_L \frac{R_{eq1} + R_{eq2}}{2}$$

- IF $W_p = W_n = W \Rightarrow C_L \simeq 4LC_{ox}W$

$$t_{av} \simeq 1.2 \times 4C_{ox}LW \times \frac{1}{2}\left[\frac{2.5}{k_n \frac{W}{L}(V_{DD} - V_{tn})} + \frac{2.5}{k_p \frac{W}{L}(V_{DD} + V_{tp})}\right]$$

$\therefore t_{av}$ INDEPENDENT OF W → BETTER MAKE $W = W_{min}$

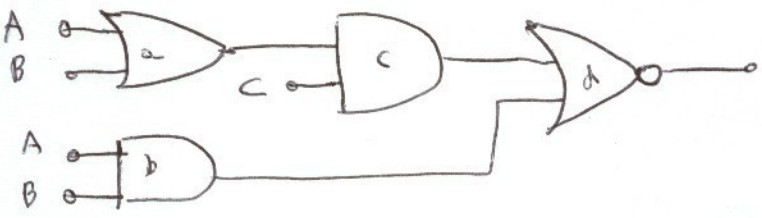
- IF ROUTING OR SIDEWALL CAPACITANCES ARE IMPORTANT, THEN INCREASING W REDUCES t_{av}
- CAN DELAY BE OPTIMIZED AS A FUNCTION OF $\frac{W_p}{W_n}$?

$$\left(\frac{W_p}{W_n}\right)_{OPT} = \sqrt{\frac{\mu_n}{\mu_p}}$$ (BY TAKING $\frac{dt_{av}}{d(\frac{W_p}{W_n})} = 0$ AND ASSUMING $|V_{tp}| = V_{tn}$)

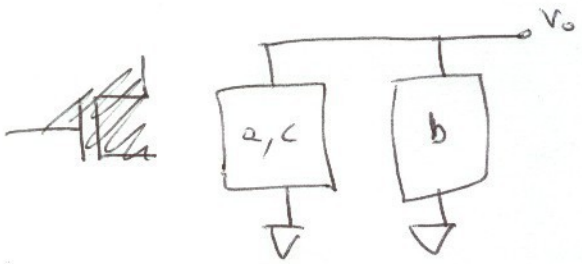
- $\sqrt{\frac{\mu_n}{\mu_p}}$ TYPICALLY $= 1.5$
- THE AVERAGE DELAY INCREASES ONLY AROUND 5% IF $\frac{W_p}{W_n} = 1$, SO FREQUENTLY THIS IS USED TO SAVE SPACE
- AGAIN, IF ROUTING OR LOADING CAPS DOMINATE $W_p > W_n$ IS ALWAYS BETTER.

CMOS GATE DESIGN

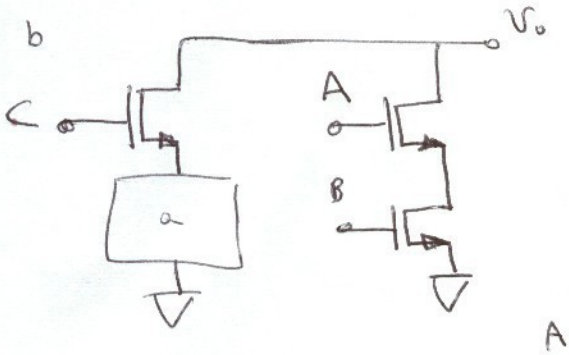
EXAMPLE:

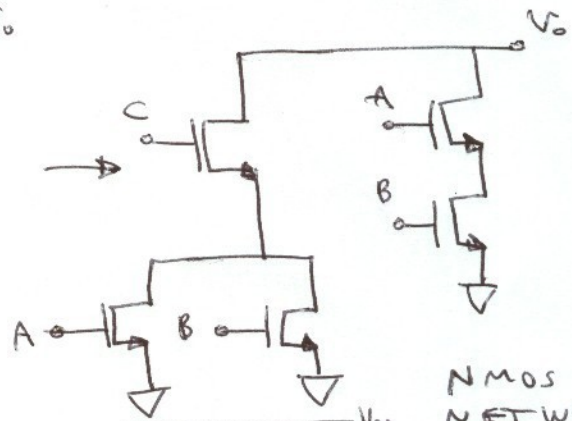


- FIRST: IMPLEMENT d:



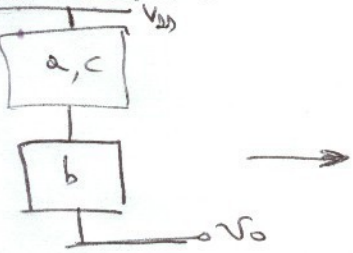
- THEN b AND c

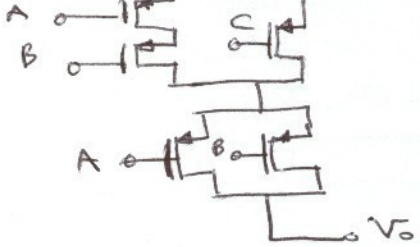




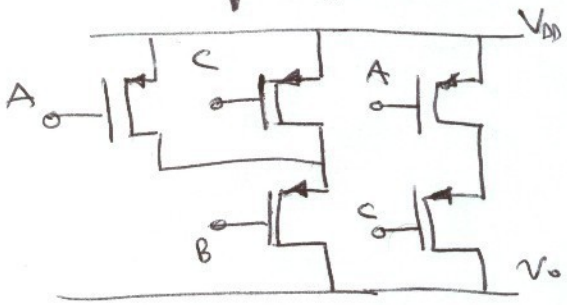
NMOS NETWORK

- PMOS; DO COMPLEMENT:

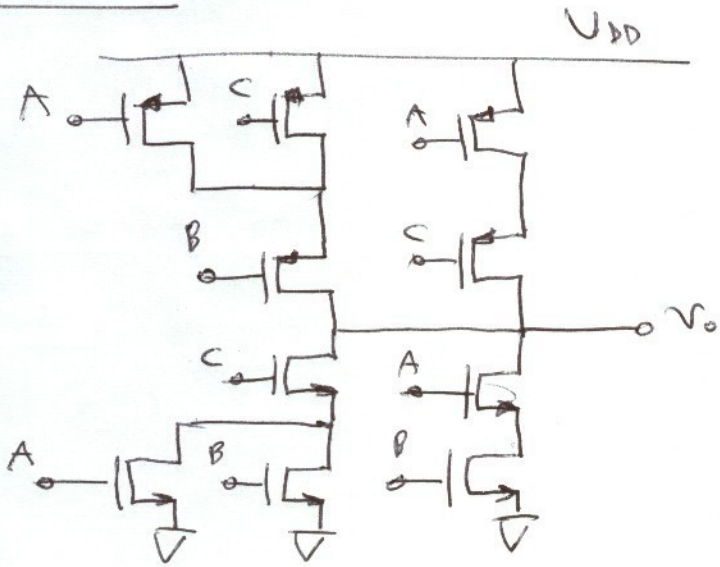




NOTE: CAN BE SIMPLIFIED BUT THERE IS NO AUTOMATIC WAY.



COMPLETE GATE

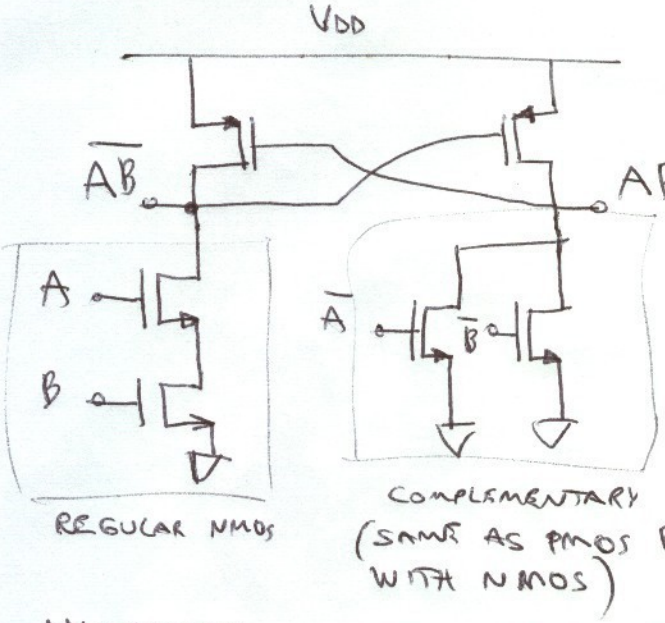


- NOTE: WORST DELAY HAPPENS ~~WHEN~~ WHEN INPUTS PRODUCE MOST TRANSISTORS IN SERIES.

SERIES → ADD Ls
PARALLEL → ADD Ws

- EQUIVALENT RESISTANCE PROPORTIONAL TO $\frac{1}{(\frac{W}{L})_{eq}}$.

DIFFERENTIAL CMOS



AND FUNCTION

ADVANTAGES:

- FEW PMOS TRANSISTORS
- NO INVERTERS NECESSARY → ELIMINATE DELAYS AND SAVE SPACE.
- FREQUENTLY LESS AREA. (BUT ROUTING MAY BE MORE DIFFICULT)
- LESS SENSITIVE TO NOISE.

OBSERVATION: NMOS NETWORKS MUST BE ABLE TO PULL DOWN VOLTAGE OF CONDUCTING PMOS.