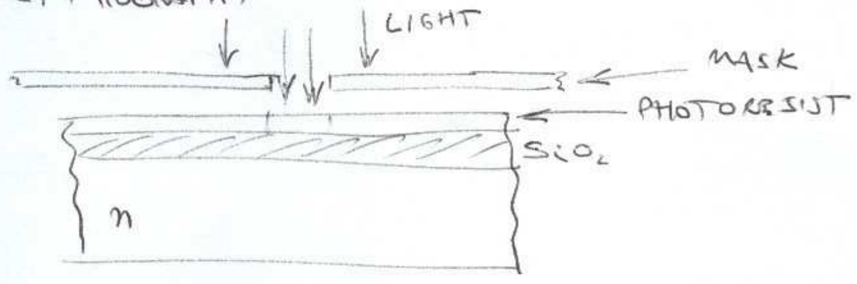
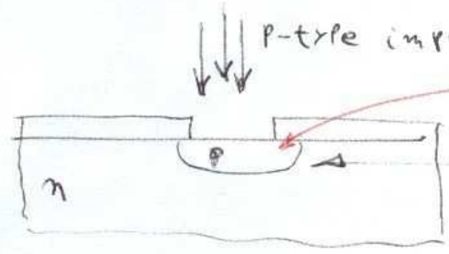
FABRICATION PROCESS (CH-2)

§ 2.2.2, 2.2.3, 2.2.4–8
§ 2.3

1) FABRICATION TECHNIQUES

• PHOTOLITHOGRAPHY

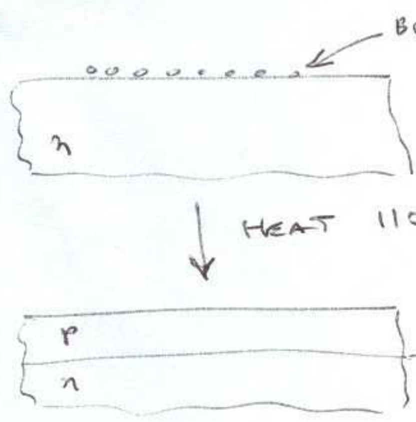




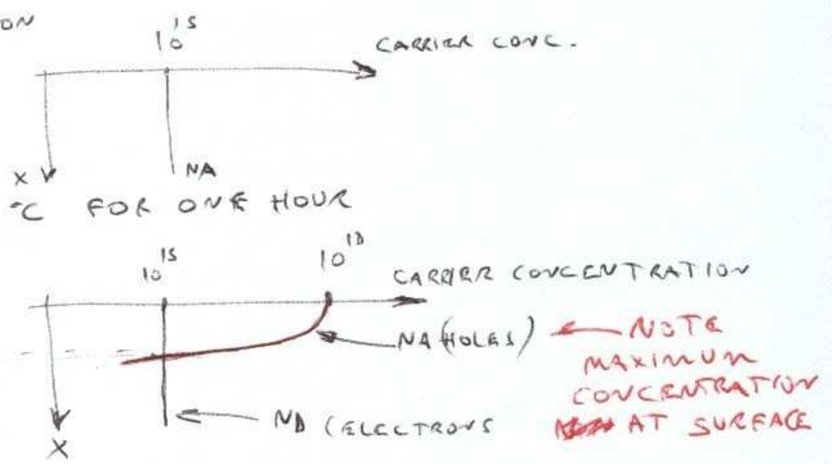
NOTE LATERAL DIFFUSION

CAN BE ACHIEVED BY
- SOLID-STATE DIFFUSION
- ION IMPLANTATION

• SOLID-STATE DIFFUSION



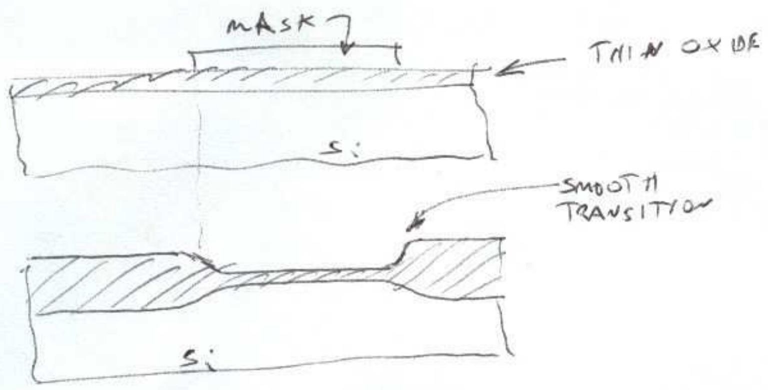
HEAT 1100 °C FOR ONE HOUR



• ION IMPLANTATION

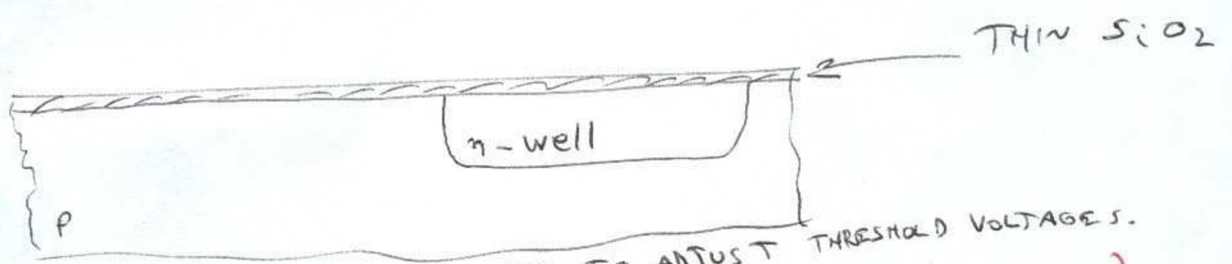
IONS ARE DIRECTED AT HIGH VELOCITY TO THE SILICON. THEY PENETRATE THE SURFACE TO A DEPTH <0.1 μm TO 0.6 μm. THEN THE SAMPLE IS HEATED TO ALLOW THE IONS TO ANNEAL WITH THE CRYSTAL STRUCTURE. → BETTER THAN DIFFUSION BECAUSE IMPURITIES CAN BE BETTER CONTROLLED AND MAX. CONCENTRATION DEPTH CAN ALSO BE CONTROLLED.

- LOCAL OXIDATION

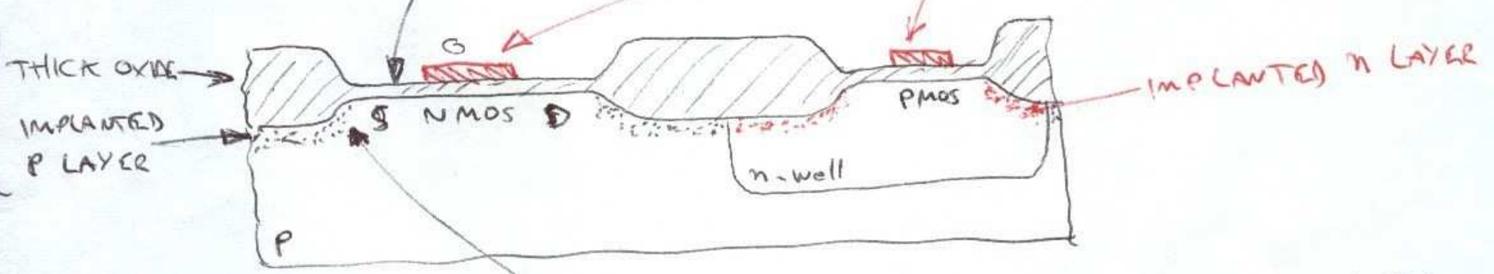


- POLYSILICON DEPOSITION
  - DEPOSIT POLY LAYER
  - ETCH MASK AND REMOVE UNWANTED PARTS (AS WITH SiO_2)

2) CMOS PROCESS (SAMPLE)

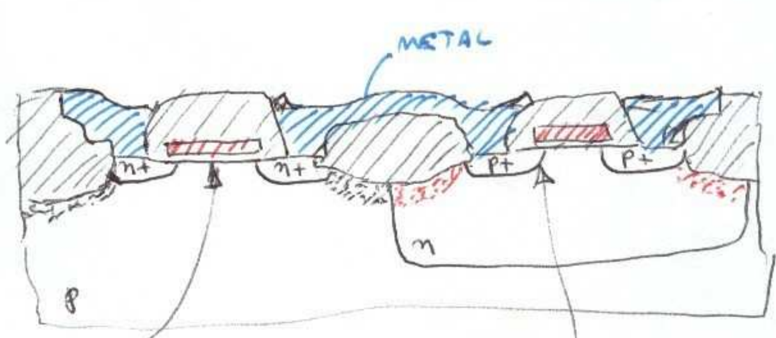


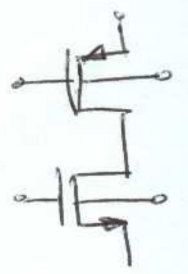
THIN OXIDE IS IMPLANTED TO ADJUST THRESHOLD VOLTAGES.



PREVENT THE FORMATION OF TRANSISTORS WITH REGULAR METAL AND POLY TRACES (V_t BECOMES HIGHER THAN SUPPLY VOLTAGE)

NOTE THE MATERIAL AROUND THE DRAIN AND SOURCE EXTERNAL PERIMETER IS DIFFERENT THAN THE SUBSTRATE.





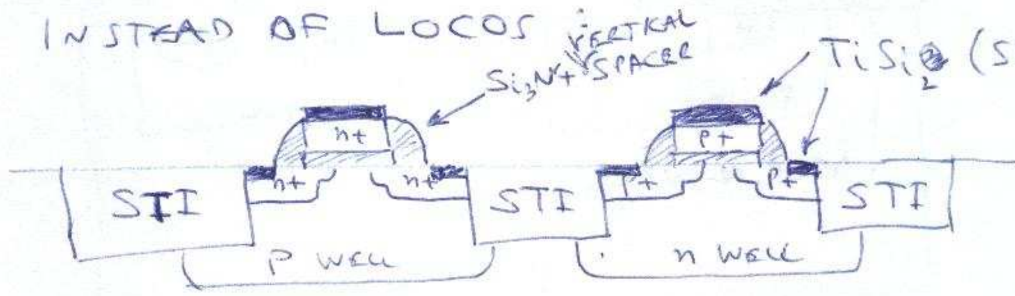
THIN OXIDE ONLY UNDER GATE

NOTE G-D AND G-S OVERLAP.

DEEP-SUBMICRON PROCESS DIFFERENCES

(250, 180, 130, 90, 65 nm)

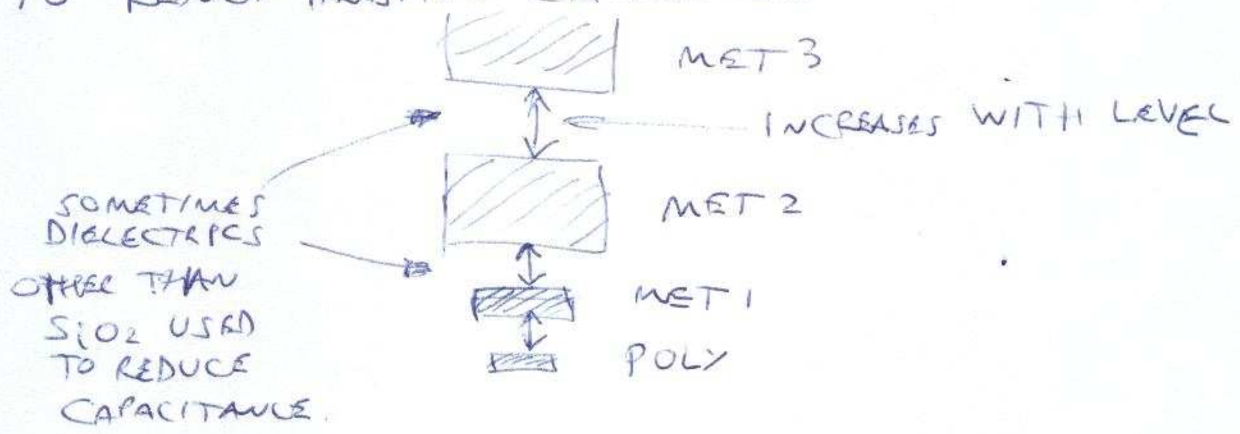
- DEVICES ISOLATED BY SHALLOW TRENCH ISOLATION (STI) INSTEAD OF LOCOS



- n+ POLY FOR NMOS, p+ POLY FOR PMOS
- SHALLOW - SOURCE-DRAIN EXTENSIONS USED TO REDUCE SHORT-CHANNEL EFFECTS
- SILICIDED SOURCE, DRAIN AN GATES TO REDUCE SHEET RESISTANCES (SALICIDATION)

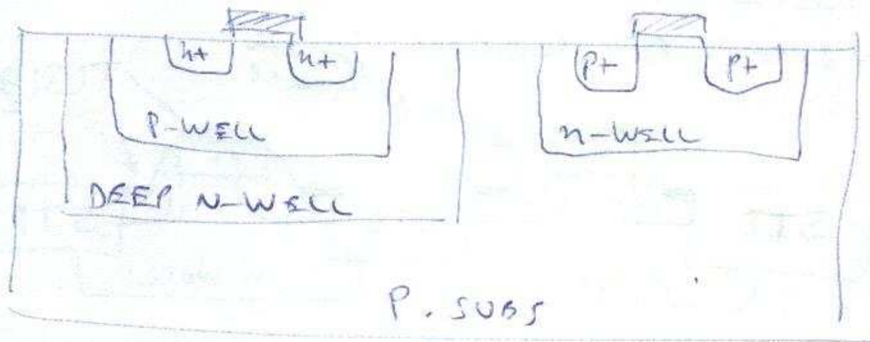
INTERCONNECTIONS

- CONVENTIONAL METALLIZATION USES Al AND TUNGSTEN TO PLUG-IN CONTACT HOLES.
- MULTI-LAYER INTERCONNECTIONS USE THICKER TRACES IN UPPER LAYERS AND HIGHER LAYER SEPARATIONS TO REDUCE PARASITIC CAPACITANCES



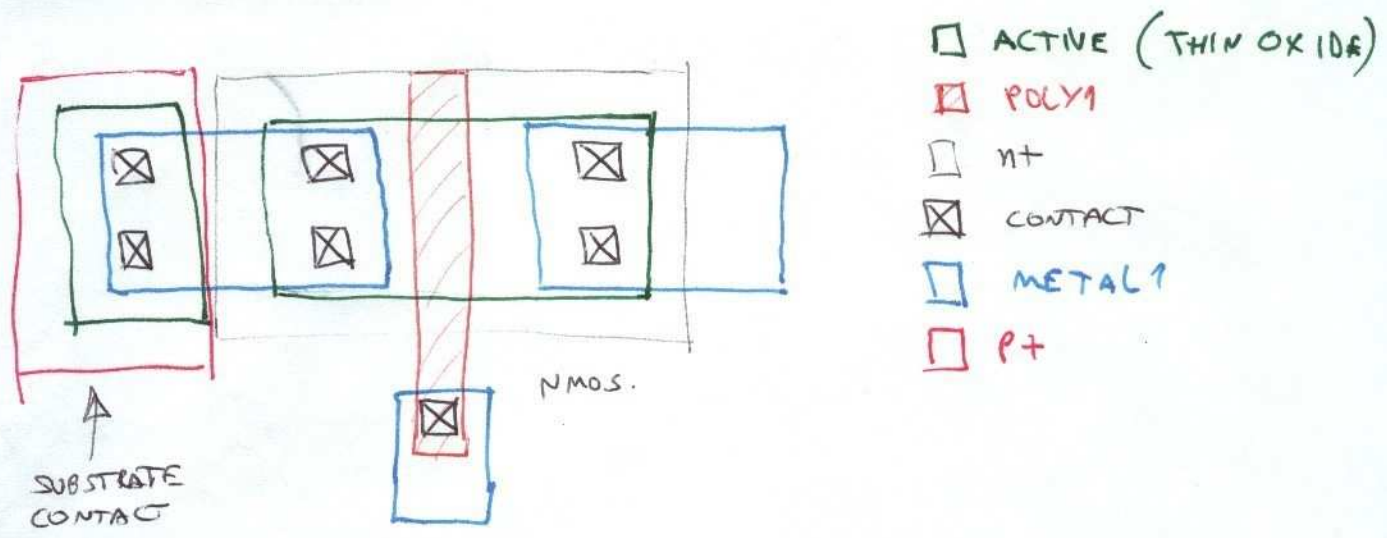
(SHOW MAIN PARAMETERS FROM BOOK)

TRIPLE-WELL PROCESS (REQUIRES EXTRA MASK)



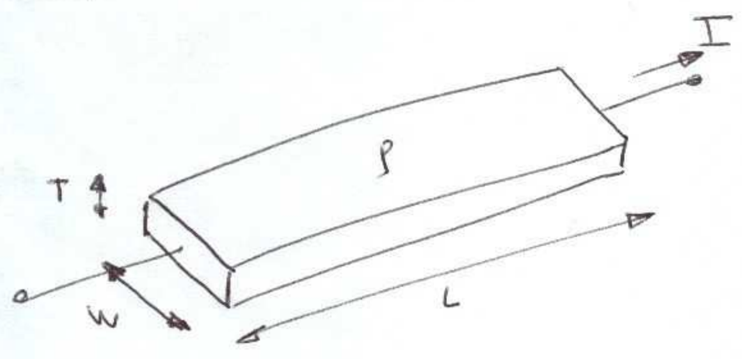
ADVANTAGE: BETTER ISOLATION BETWEEN TRANSISTORS AND SUBSTRATE. ALSO ALLOWS ~~FLOATING~~ NON-GROUNDED SUBSTRATES FOR NMOS DEVICES.

~~RESISTIVITY~~ MOS TRANSISTOR LAYOUT



- PMOS IS SIMILAR WITH THE ADDITION OF NWELL
- NORMALLY WE WANT TO MINIMIZE AREA → REDUCE COST.

RESISTIVITY OF DIFFUSED LAYERS



$$R = \rho \frac{L}{WT} = \left(\frac{\rho}{T}\right)\frac{L}{W}$$

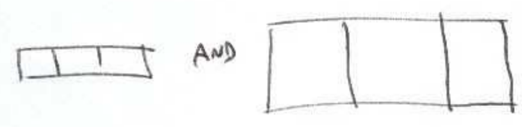
($\frac{L}{W}$ CAN BE CHANGED IN LAYOUT)

$$R = R_{\square}\frac{L}{W}$$

$$R_{\square} := \frac{\rho}{T} \quad \left(\frac{\Omega}{\square}\right)$$

EXAMPLE: $L = 50\mu m$, $W = 5\mu m$, $R_{\square} = 200\frac{\Omega}{\square}$

$$\frac{L}{W} = 10\,\square \qquad R = 10\square \times 200\frac{\Omega}{\square} = 2k\Omega$$

NOTE:  HAVE SAME RESISTANCE

EFFECTIVE CHANNEL LENGTH

$$L_{eff} = L_{drawn} - 2L_d$$, L_d : LATERAL DIFFUSION LENGTH

EXAMPLE: 0.4μm PROCESS: $L_{drawn} = 0.4\mu m$, $L_d = 0.09\mu m$

∴ ADD $2 \times L_d$ TO EFFECTIVE LENGTH IN CALCULATIONS

$$I_d = \frac{k'}{2}\frac{W}{L_{eff}}(V_{GS}-V_t)^2$$

L_{eff} ← SHOULD BE USED ALWAYS.

SERIES DRAIN / SOURCE RESISTANCE

$$R_d = NRD \times R_{SH}$$
$$R_s = NRS \times R_{SH}$$

R_{SH} : SHEET RESISTANCE OF DRAIN/SOURCE $\left(\frac{\Omega}{\square}\right)$

NRS, NRD : NUMBER OF SQUARES IN DRAIN / SOURCE.

- INTRINSIC CAPACITANCE (ACTIVE REGION)

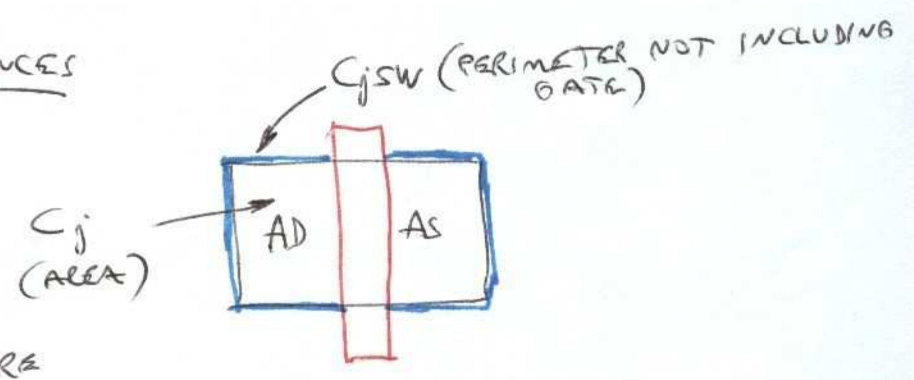
$$C_{gs} = \frac{2}{3} W L_{eff} C_{ox}$$

- OVERLAP CAPACITANCE

$$C_{OL} = W L_d C_{ox}$$

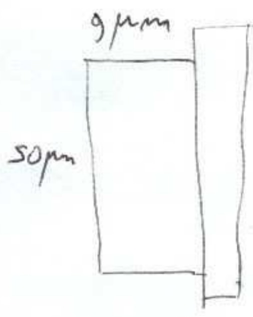
TOTAL:
- GATE-SOURCE : $C_{gs} + C_{OL}$
- GATE-DRAIN : C_{OL}

JUNCTION CAPACITANCES



. THESE CAPACITANCES ARE BIAS-DEPENDENT.

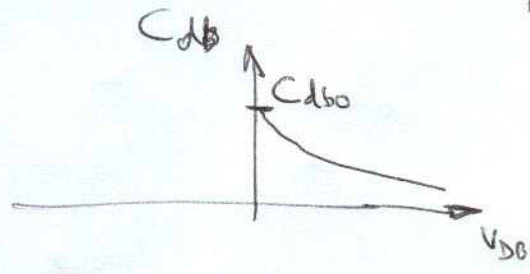
EXAMPLE:



$C_{jsw0} = 0.5 \frac{fF}{\mu m}$

$C_{j0} = 0.08 \frac{fF}{(\mu m)^2}$

$C_{jsw} = 34fF$, $C_j = 36fF$ } $C_{db0} = 70fF$ ← ZERO BIAS



$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{\psi_0}}}$$

ψ_0 ← JUNCTION POTENTIAL (ASSUME 0.65V)

$C_{db}(5V) = 24fF$

RESISTORS

- DIFFUSED RESISTORS

- POLY RESISTORS
- WELL RESISTORS
- MOS DEVICES IN TRIODE REGION:

$$R = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{L}{W} \underbrace{\frac{1}{k'(V_{GS} - V_t - V_{DS})}}_{R_\square}$$

$$R_\square = \frac{1}{k'(V_{GS} - V_t - V_{DS})}$$

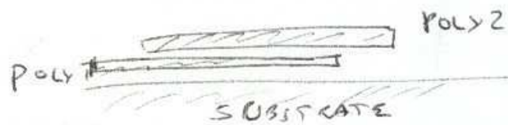
$R_\square$ ← OF CHANNEL

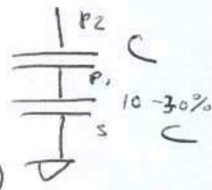
DEPENDS ON V_{DS} BUT OK IF $V_{DS} \ll V_{OV}$

(ADD CAPACITORS, LATCH-UP, DETERMINATION OF PARAMETERS)

CAPACITORS

- POLY-POLY CAPACITORS





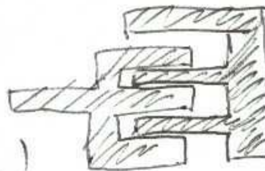
(BUT COULD BE ISOLATED WELL)

- MATCHING UP TO 0.05% IN SAME IC.

- MOS TRANSISTOR GATES → NONLINEAR, BUT OK WHEN VALUE IS NOT CRITICAL.

- MIM CAPACITORS (METAL - INSULATOR - METAL)
  PROCESS HAS THE OPTION OF USING A THIN OXIDE BETWEEN 2 METAL LAYERS
  CMOS018 → METAL 5 AND METAL 6 (CTM IS THIN OXIDE)

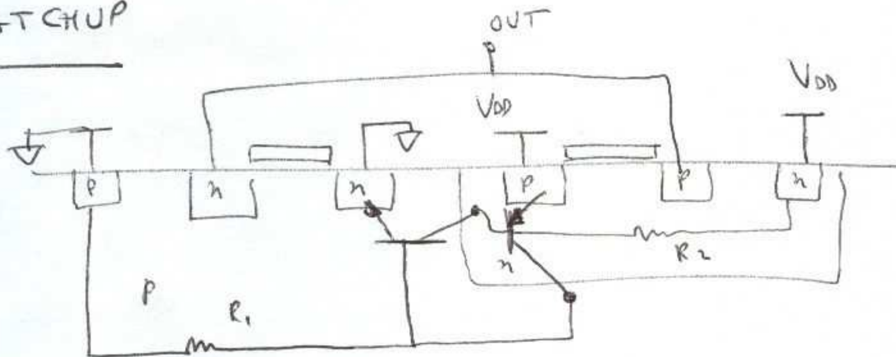
- LATERAL CAPACITORS



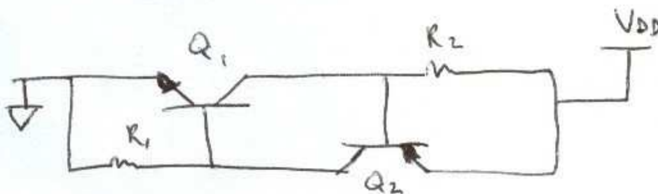
SAME LAYER.

(LESS AREA IN WITH SMALL GEOMETRY TECHNOLOGIES.)

LATCHUP



INVERTER



- INITIALLY Q_1, Q_2 ARE CUT OFF.
- IF CURRENT IS INJECTED IN SUBSTRATE (DUE TO A TRANSIENT, FOR EXAMPLE), VOLTAGE DROP IN R_1 CAN TURN ON Q_1 → PRODUCES CURRENT IN R_2 → TURNS ON Q_2 → SHORT CIRCUIT BETWEEN V_{DD} AND GROUND (LATCH UP)
- SOLUTION IS TO PUT MANY SUBSTRATE/WELL CONTACTS TO REDUCE R_1, R_2.