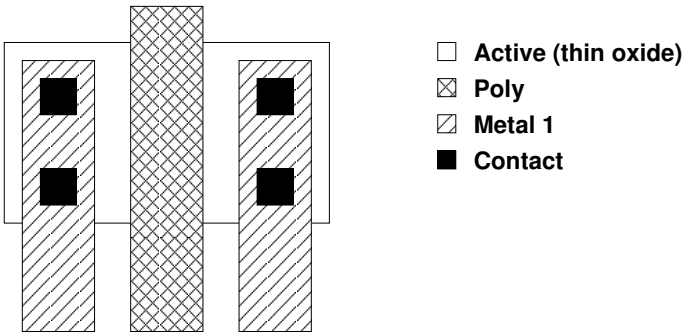
# EELE 5131
# Practice Problems for Midterm — Winter 2019

Parameters for all problems: $I_{SQn} = 280$ nA, $V_{thn} = 0.5$ V, $|\partial L/\partial V_{DS}|_n = 0.03$ $\mu$m/V, $I_{SQp} = 80$ nA, $V_{thp} = -0.55$ V, $|\partial L/\partial V_{DS}|_p = 0.04$ $\mu$m/V, $n_n = n_p = 1.3$, $t_{OX} = 6$ nm and $A_\beta = 3$ %$\mu$m.

## Problems and Questions

1. The following layout is for a transistor in a process with p-type substrate.

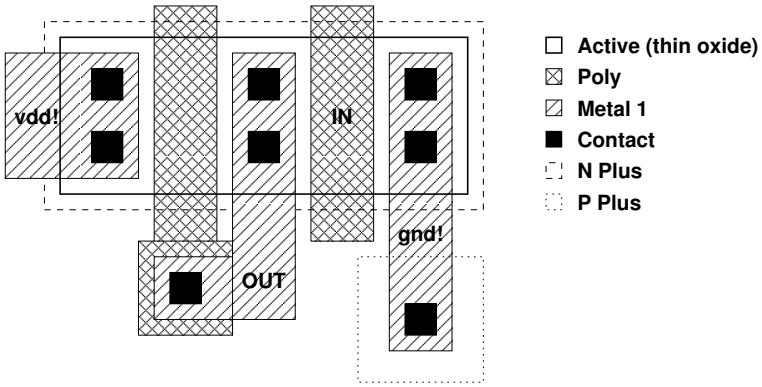
   - What layer is missing to form an NMOS transistor?
   - What layers are missing to form a PMOS transistor instead?




   Answers: (a) n+, (b) p+ and N-well

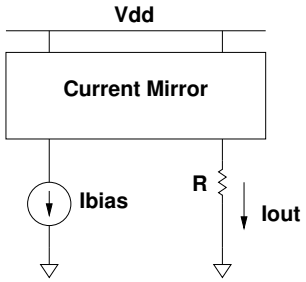
2. The following layout is for a process with p-type substrate.

   - Draw an schematic diagram of the circuit in this layout. Use the provided node labels.
   - Is there any missing layer(s) and if yes and where? (mark in the figure and explain).




   Answer: (b) Active layer missing in substrate contact

3. A 1:1 PMOS mirror is designed with 2 unit transistors with $(W/L) = (10\mu\text{m}/1\mu\text{m})$. The mirror is connected as shown below. The load resistor is $R = 10$ k$\Omega$ and the supply voltage is 1.8 V.




   (a) Draw a current mirror schematic. Include input current source, load resistor and bulk connections.

   (b) Calculate the source-drain voltage in each transistor for the following values of $I_{BIAS}$: 25 nA, 5 $\mu$A and 40 $\mu$A.

   (c) Estimate the maximum load voltage and the output resistance of the mirror for $I_{BIAS} = 40$ $\mu$A.

   (d) Calculate the standard deviation (in %) in output current when $I_{BIAS} = 5$ $\mu$A separately due to threshold voltage mismatch alone, specific current mismatch alone and the two combined.

4. Design a simple PMOS current mirror subject to the following specifications:

   - Supply voltage is 3 V.
   - The operating output voltage range must be from zero up to 2.75 V.
   - The input and output currents are equal to 60 $\mu$A.
   - The output current must change by 3 % or less with a decrease of 1 V in the output voltage ($V_{out}$).
   - Minimize gate area as much as possible.

   Show the schematic with transistor dimensions for full marks.

5. Re-design the previous current source for an input current of 240 $\mu$A and an output current of 30 $\mu$A. Use unit transistors for good matching.

   Answer: use the same design as in (3), with 4 units in parallel for input branch and two in series for output branch.

6. Calculate the resistor needed to generate the input current in Problem 5.

7. Neglecting channel-length modulation, estimate the difference between the input and output currents in your design in Problem 4 when $V_{th}$ mismatch between transistors is 15 mV.

8. Design a simple NMOS current mirror subject to the following specifications:

   (a) Supply voltage is 3.3 V.

   (b) The mirror must operate correctly with an output voltage of at least 0.25 V.

   (c) The input current is 60 $\mu$A and output current is 90 $\mu$A.

   (d) The output current must change by 2 % or less with an increase of 1 V in the output voltage ($V_{out}$).

   (e) Minimize gate area as much as possible. Assume that due to matching requirements, minimum gate dimension is 1 $\mu$m.

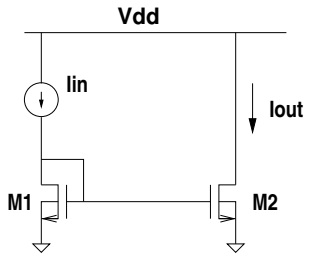
   Show schematic and unit transistor dimensions for full marks.

9. Neglecting channel-length modulation, estimate the difference between the input and output currents in your design of the previous problem when $V_{th}$ mismatch between transistors is 5 mV.

10. In the figure, $I_{in} = 20$ $\mu$A, $V_{DD} = 2.5$ V and $(W/L)_1 = (W/L)_2 = (2\mu\text{m}/2\mu\text{m})$.

    (a) Calculate $I_{out}$ considering the effect of channel-length modulation, assuming perfect matching. Show calculation steps.

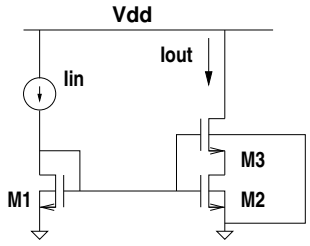
    (b) Neglecting channel-length modulation, estimate the standard deviation in output current due to transistor mismatch.



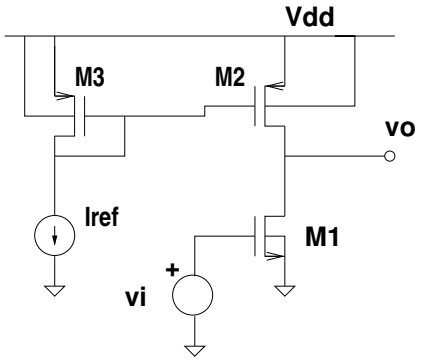

11. In the figure, $I_{in} = 0.5$ $\mu$A, $V_{DD} = 3$ V and all transistors are equal with $(W/L) = 20$. Justify your answers.

    (a) Specify regions of operation for each of M1, M2 and M3: inversion level (weak, moderate or strong) and triode or active.

    (b) Neglecting channel-length modulation calculate $i_{f2}$ and $i_{r2}$.



12. In the figure below, $V_{DD} = 1.6$ V, $I_{ref} = 50$ $\mu$A, $(W/L)_1 = (20\mu\text{m}/1\mu\text{m})$ and $(W/L)_2 = 3(W/L)_3 = (10\mu\text{m}/1\mu\text{m})$.




(a) Calculate the DC voltage required at the input to bias the amplifier in the high-gain region.

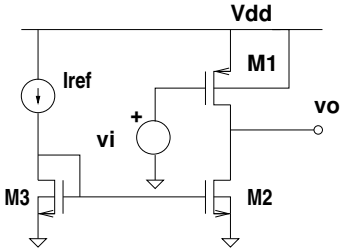
(b) Calculate the output voltage range for high gain.

(c) Calculate the transconductance of M1.

(d) Calculate the output resistance of the amplifier.

(e) Calculate the small-signal gain of the amplifier.

13. Design a CS amplifier with current-mirror load as shown in the figure for a gain of at least 180 and an output voltage swing of at least $\pm 0.5$ V. The supply voltage is $V_{DD} = 1.8$ V, the reference current is 50 $\mu$A and $L \geq 1$ $\mu$m for all transistors. Try to minimize area.




14. Calculate the output resistance of your designed amplifier.