ENGI 5131
Midterm Sample Problems — Winter 2013

ACM parameters: $I_{SQn} = 280$ nA, $V_{thn} = 0.5$ V, $|\partial L/\partial V_{DS}|_n = 0.03$ μm/V, $I_{SQp} = 80$ nA, $V_{thp} = -0.55$ V, $|\partial L/\partial V_{DS}|_p = 0.04$ μm/V, $L_D = 0$ and $n_n = n_p = 1.31$.

Problems and Questions

1. Design a simple PMOS current mirror subject to the following specifications:

   - Supply voltage is 3 V.
   - The operating output voltage range must be from zero up to 2.75 V.
   - The input and output currents are equal to 60 μA.
   - The output current must change by 3 % or less with a decrease of 1 V in the output voltage (V_{out}).
   - Minimize gate area as much as possible.

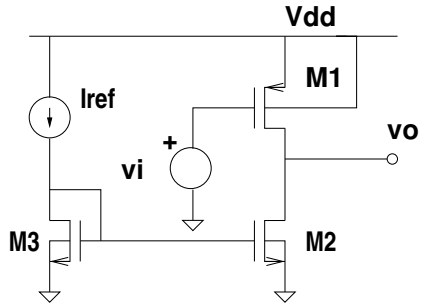
   Show the schematic with transistor dimensions for full marks.

2. Re-design the previous current source for an input current of 200 μA and an output current of 50 μA. Use unit transistors for good matching.

3. Calculate the resistor needed to generate the input current in Problem 2.

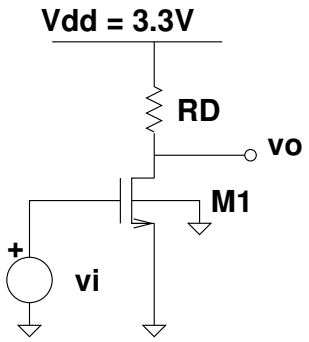
4. Neglecting channel-length modulation, estimate the difference between the input and output currents in your design in Problem 1 when V_{th} mismatch between transistors is 15 mV.

5. Design a CS amplifier with current-mirror load as shown in the figure for a gain of at least 180 and an output voltage swing of at least ± 1 V. The supply voltage is $V_{DD} = 3$ V, the reference current is 100 μA and $L \geq 1$ μm for all transistors. Try to minimize area.

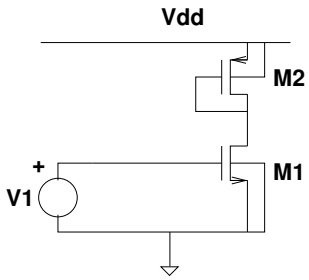


6. Calculate the DC input voltage required in the amplifier that you designed in the previous problem.

7. In the amplifier shown below, what is the maximum small-signal gain that can be achieved? Justify your answer. You are free to adjust all other circuit parameters.



8. Given $(W/L)_2 = 0.5$, $V_{DS1} = 0.2$ V and $V_{DD} = 3$ V, calculate what is the maximum gain that can be achieved by the circuit shown below:



9. For an inverter with minimum gate length (0.4 μm) and $W_p = 5$ μm, estimate W_n for a threshold voltage equal to 1.5 V with a supply voltage of 3 V (you can use strong inversion equations).

10. The following layout is for a transistor in a process with p-type substrate.

    - What layer is missing to form an NMOS transistor?
    - What layers are missing to form a PMOS transistor instead?