EELE 5131
Practice Problems for Final Exam — Winter 2019

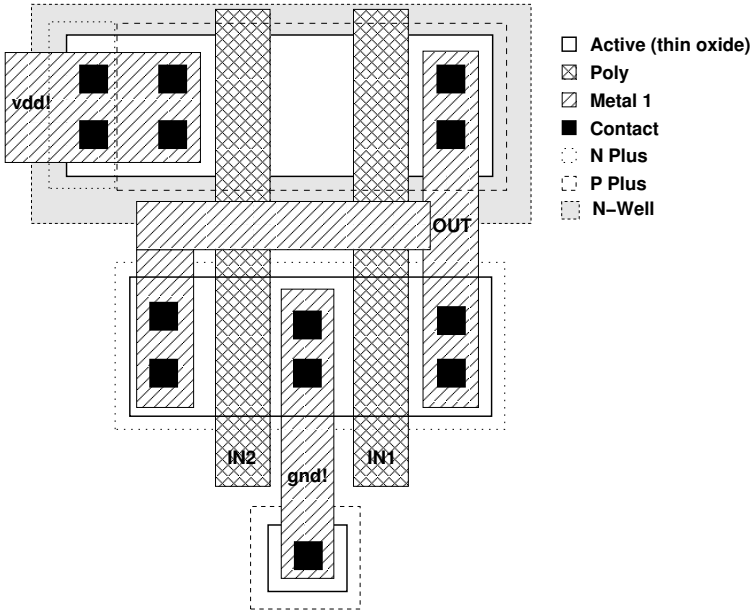
Parameters for all problems: $I_{SQn} = 280$ nA, $V_{thn} = 0.5$ V, $|\partial L/\partial V_{DS}|_n = 0.03$ μm/V, $I_{SQp} = 80$ nA, $V_{thp} = -0.55$ V, $|\partial L/\partial V_{DS}|_p = 0.04$ μm/V, $n_n = n_p = 1.3$, $t_{OX} = 6$ nm and $A_\beta = 3$ %μm. Minimum allowed dimension for analog circuits is 1 μm.

1. Design a cascode high-swing current mirror using the least possible gate area. Supply voltage is 2.8 V. Input current is 2 μA, output current is 10 μA. Output voltage range is 500 mV – 2.8 V. Current mismatch due to channel-length modulation should be no more than 1%. All transistors must be implemented by combinations of a unit transistor.

   - Specify inversion levels for the transistors in each branch.
   - For each transistor, specify aspect ratio (W/L) and number of unit transistors in series/parallel.

2. Repeat the previous problem for a PMOS mirror with an output voltage range of 0–2.3 V.

3. The following layout is for a process with p-type substrate. Draw an schematic diagram of the circuit in this layout. Show transistor substrate connections and node labels in the schematic.



4. The differential amplifier shown in the figure has been designed to operate as follows: $i_{f1} = i_{f2} = 15$, $i_{f3} = i_{f4} = 140$, $i_{f5} = 200$. Assume all transistors have $L = 1.5$ μm. Other circuit paramenters: $V_{DD} = 1.8$ V, $C_L = 0.5$ pF. Make reasonable assumptions for any missing data. Justify your answers and derive expressions for full marks.

   (a) Calculate the input common-mode voltage range.

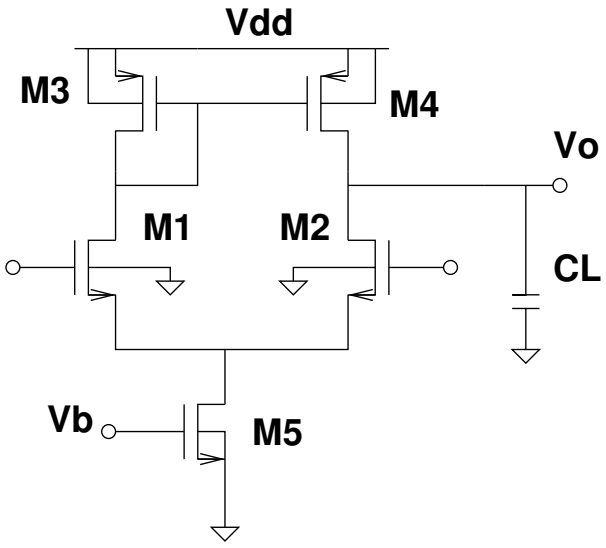
   (b) Calculate the output voltage range when the input common-mode voltage is 1.1 V

   (c) Calculate the differential voltage gain.

   (d) Calculate the CMRR assuming perfect matching.

   (e) Calculate the -3 dB bandwidth of the amplifier (assuming it is driven by a differential ideal voltage source).

   (f) Calculate all transistor widths for a slew rate equal to 200 V/μs.



5. Repeat the previous problem but use a complementary amplifier: PMOS source coupled input with an NMOS current mirror load. Draw schematic first. For part (b) assume the input common-mode voltage is 0.5 V.

6. The differential amplifier shown in the figure has been designed to operate as follows: $i_{f1} = i_{f2} = 20$, $i_{f3} = i_{f4} = 100$, $i_{f5} = 150$. Assume all transistors have the same channel length, $L = 1$ μm and $M_3 \equiv M_{3'}$, $M_4 \equiv M_{4'}$ and $M_5 \equiv M_{5'}$. Supply voltages are $V_{DD} = V_{SS} = 0.9$ V.

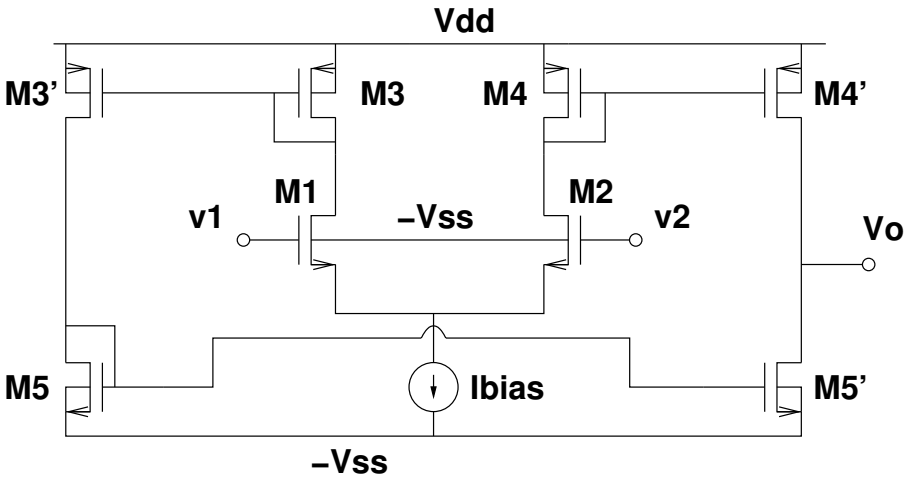
   (a) Calculate the differential-mode gain.

   (b) Calculate the input common-mode voltage range. Assume the current source (I_{BIAS}) needs at least 0.22 V to work.

   (c) Calculate the output voltage range.

   (d) Calculate all transistor widths if $I_{BIAS} = 50$ μA.

   (e) Calculate the amplifier maximum slew-rate with a load capacitance of 1 pF.



7. Which answers change in the previous problem if $(W/L)_{4'} = 2(W/L)_4$ and $(W/L)_{3'} = 2(W/L)_3$? Calculate the new answer(s).

8. Repeat part (b) of the previous problem for the complementary amplifier (exchange NMOS and PMOS and invert supply voltages).

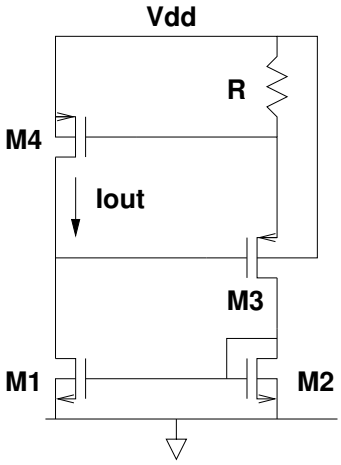
9. For an inverter with $L = 0.2$ μm for both transistors and $W_n = 1$ μm, estimate W_p for a threshold voltage equal to 0.45 V with a supply voltage of 1.6 V. Neglect short-channel effects but note that one of the transistors is not in strong inversion at the threshold.

10. Estimate the rise and fall times of the inverter of the previous problem when it is loaded with a 0.2 pF capacitor.

11. The current source of the figure requires all transistors to operate in active mode. $(W/L)_1 = (W/L)_2 = 1$, $(W/L)_3 = 2$, the desired output current is 1 μA with M4 operating with an inversion level $i_{f4} = 20$.

    (a) Find the resistor value and $(W/L)_4$

    (b) Calculate the minimum V_{DD} required by this circuit.



12. In the figure, $(W/L)_2 = 40(W/L)_1 = 1.2$, and the desired output current at room temperature is 1 μA.

    (a) Calculate the voltage drop at the resistor at room temperature.

    (b) Calculate the resistor value.

    (c) Calculate the output current at 0°C.