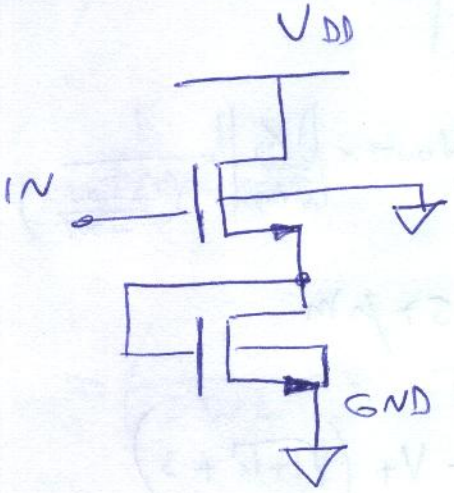
EELE 5131 : SOLUTIONS TO ASSIGNMENT #3 (2019)

1)



(MAKE SURE SUBSTRATE CONTACTS ARE SHOWN)

2) $I_{in} = 3\mu A$, $I_{OUT} = 2\mu A$ $\quad \frac{I_{OUT}}{I_{in}} = \frac{2}{3}$

$V_{DD} = 1.8\,V$

$V_{OUT\,max} = 1.6\,V$ (PMOS MIRROR)

$\sigma\left(\frac{\Delta I_o}{I_o}\right)$ DUE TO MISMATCH $\leq 2\%$

$A_{VT} = 4.1\,mV\mu m$, $A_\beta = 0.03/\mu m$

$\frac{\Delta I_o}{I_o} \leq 3\%$ FOR $\Delta V_{OUT} = 1V$

- MINIMIZE GATE AREA

- PMOS PARAMETERS FROM TUTORIAL:

$V_{th} = -438\,mV$

$I_{sq} = 1.13 \times 28.84\,nA = \underline{32.6\,nA}$

$n \simeq 1.32$

$\left|\frac{\partial \lambda_D}{\partial V_{DS}}\right| = \frac{10\mu m}{290\,nA} \times \frac{0.8\,mA}{200\,mV} = 0.137\,\frac{\mu m}{V}$

(2)

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} \leq r_o = \frac{L_{eff}}{I_{OUT} \times \left|\frac{\partial X_D}{\partial V_{DS}}\right|} \qquad (1)$$

~~$\frac{\Delta I_{OUT}}{I_{OUT}} \frac{\Delta V_{OUT}}{}$~~ $L_{eff} \geq \Delta V_{OUT} \times \left|\frac{\partial X_D}{\partial V_{DS}}\right| \cdot \frac{1}{\left(\frac{\Delta I_{OUT}}{I_{OUT}}\right)}$

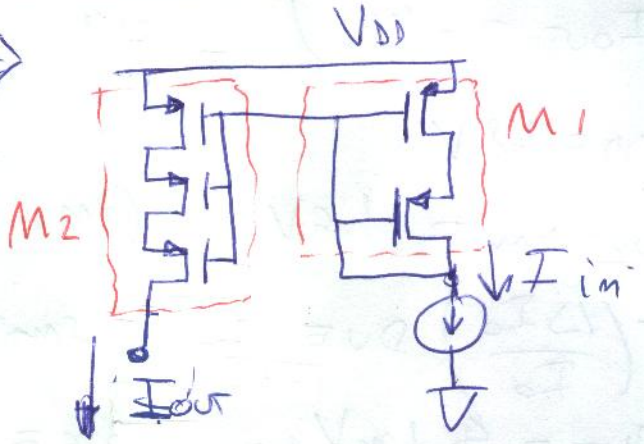
(1) $L_{eff} \geq 4.57\,\mu m$

(2) $V_{OUT\,MAX} = V_{DD} - V_{DS_{SAT}} = V_{DD} - V_T\left(\sqrt{1+i_f} + 3\right)$

$$i_{f_{MAX}} = \left(\frac{V_{DD} - V_{OUT_{MAX}}}{V_T} - 3\right)^2 - 1 = \underline{21.02} \qquad (2)$$

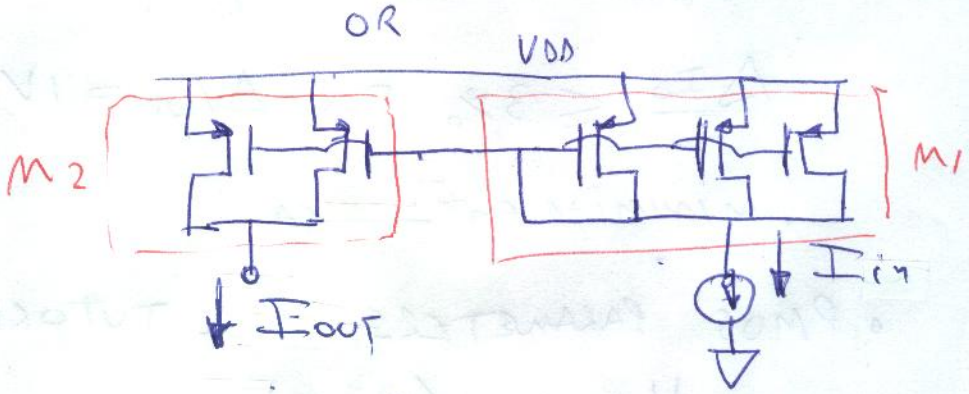
(3) FOR GAIN $= \frac{2}{3} \Rightarrow$

CIRCUIT 1



OR

CIRCUIT 2



- IN BOTH CASES, THE CURRENT GAIN MISMATCH IS GIVEN BY :

$$\sigma\left(\frac{\Delta a_i}{a_i}\right)^2 = \sigma\left(\frac{\Delta I_{in}}{I_{in}}\right)^2 + \sigma\left(\frac{\Delta I_{OUT}}{I_{OUT}}\right)^2$$

$$= \left(\frac{1}{\text{AREA OF } M_1} + \frac{1}{\text{AREA OF } M_2}\right)\left[\left(\frac{A_{VT}}{nV_T}\right)^2 \frac{\ln(1+i_f)}{i_f} + A_\beta^2\right]$$

$$= \left(\frac{1}{3WL} + \frac{1}{2WL}\right)\left[\left(\frac{A_{VT}}{nV_T}\right)^2 \frac{\ln(1+i_f)}{i_f} + A_\beta^2\right]$$

$$= \left(\frac{1}{2}+\frac{1}{3}\right)\frac{1}{WL}\left[\left(\frac{A_{VT}}{nV_T}\right)^2 \frac{\ln(1+i_f)}{i_f} + A_\beta^2\right]$$

(WL IS THE AREA OF A UNIT TRANSISTOR.)

- FOR MINIMUM AREA, CHOOSE $i_{f_{MAX}}$ FOR 2 REASONS:
  1) $I_D \propto \frac{W}{L} i_f$, GIVEN THAT L IS FIXED, A HIGHER i_f MEANS LOWER W.
  2) $\sigma\left(\frac{\Delta a_i}{a_i}\right)^2$ DECREASES WITH $i_f \Rightarrow$ LESS (WL) REQUIRED

$(WL)_{min} = 6.4\ \mu m^2$ FOR ONE UNIT TRANSISTOR

($i_f = 20$)

- TRY SERIES CONFIGURATION:

$L_{2_{eff}} \geq 4.57\mu m \Rightarrow L_2 = 6\mu m \Rightarrow L_U = 2\mu m$ (UNIT TRANSISTOR)

COULD USE $1.6\mu m$

$3 \times 1.6\mu m = 4.8\mu m$

$$I_{OUT} \cong I_{SQ} \times \frac{W_U}{3L_U} \times i_f$$

NEGLECTING C_D

(4)

$$2\mu A = 32.6nA \times \frac{W_U}{3\times 2\mu m} \times 20 \Rightarrow W_U = 18.40\mu m$$

$$\frac{W_U}{L_U} = \frac{18.40\mu m}{2\mu m}$$

FOR SERIES

$$AREA_U = 36.8\mu m^2 > 6.4\mu m^2 \text{ OK}$$

- TRY PARALLEL

$$L_U = 4.6\mu m$$

$$2\mu A = 32.6nA \times \frac{W_U \times 2}{4.6\mu m} \times 20 \Rightarrow W_U = 7.06\mu m$$

FOR PARALLEL

$$AREA_U = 32.5\mu m^2 > 6.4\mu m^2 \text{ OK}$$

∴ BOTH TOPOLOGIES GIVE ABOUT THE SAME AREA. (FOR THIS PARTICULAR SET OF VALUES)

(PARALLEL IS A LITTLE BETTER)

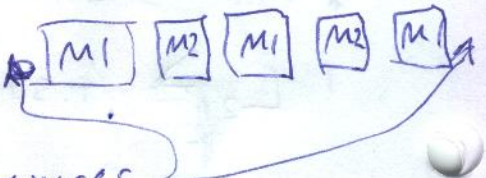
(*) ACTUALLY SERIES WITH $L_U = 1.6\mu m$ IS BETTER $AREA_U = 23.5\mu m^2$

FINAL DESIGN: • PARALLEL TOPOLOGY (CIRCUIT 2)

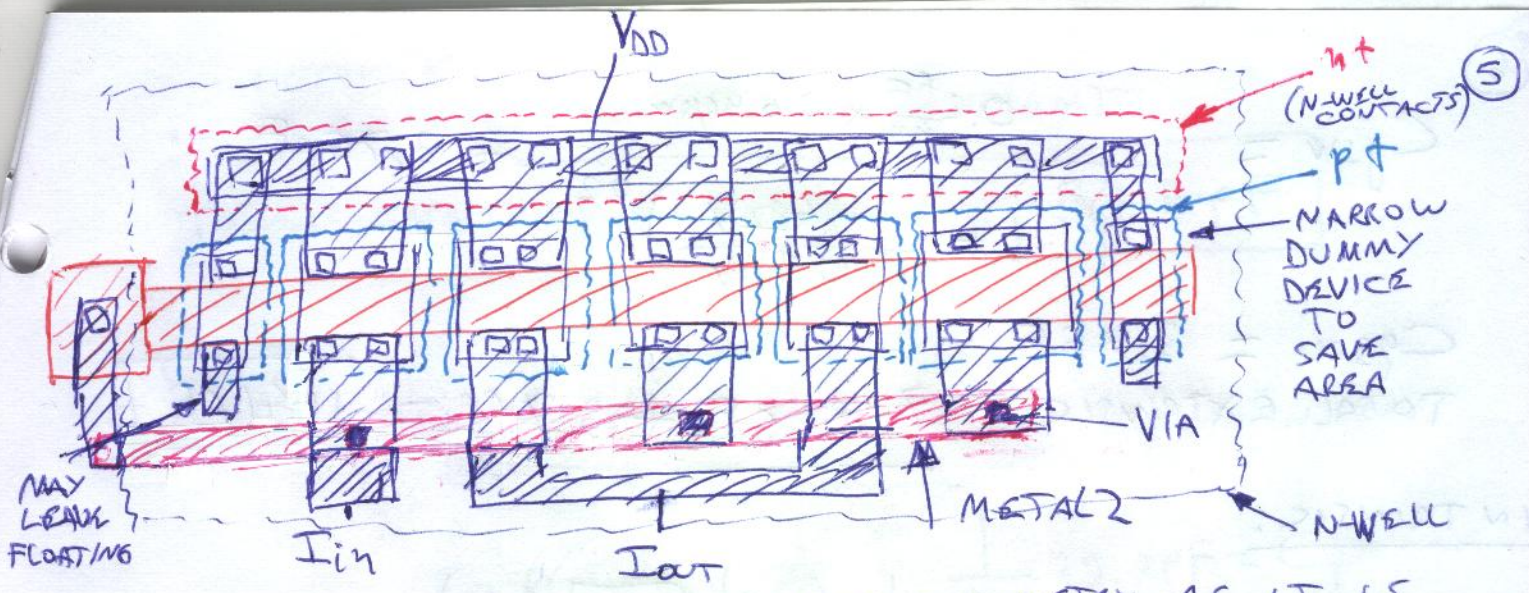
• UNIT TRANSISTOR $\frac{W_U}{L_U} = \frac{7.1\mu m}{4.6\mu m}$

3) LAYOUT SHOULD USE SOME DEVICE MATCHING TECHNIQUES:

- SAME SHAPE AND SIZE OF UNIT TRANSISTORS
- MINIMUM DISTANCE BETWEEN "
- NICE TO USE COMMON CENTROID



- SAME ORIENTATION
- SAME SURROUNDINGS: ADD DUMMY DEVICES



• NOTE: METAL 2 DOES NOT NEED SYMMETRY AS IT IS AT AN UPPER LEVEL.

4) $W = 10\mu m$

$L = 1\mu m \Rightarrow L_{eff} = 1\mu m - 2 \times 20nm = 0.96\mu m$

$AD = 0.48\mu m \times 10\mu m = 4.8\mu m^2$

$PD = (0.48 + 10\mu m) \times 2 = 20.96\mu m$

USE ACM EXTRACTED VALUES FROM TUTORIAL

$i_F = 10$, $I_{sp} \simeq 132nA$, $n \simeq 1.3$, $V_{th} = 418mV$

a) $I_D = 132nA \times \frac{10\mu m}{0.96\mu m} \times 10 \cong 14\mu A$

$V_G = V_{th} + n V_T \underbrace{q(10)}_{\sim 2.2} = 492mV$

b) EXTRINSIC:

JUNCTION CAPACITANCE:

$$C_j = \frac{1\frac{fF}{\mu m^2} \times 4.8\mu m^2}{\left(1 + \frac{0.492V}{0.69V}\right)^{0.36}} = 3.95fF$$

(6)

$$C_{jsw} = \frac{0.2\frac{fF}{\mu m} \times 20.96\mu m}{\left(1 + \frac{0.492V}{0.69V}\right)^{0.2}} = 3.76fF$$

$C_{gsov} = 3.7fF$

TOTAL EXTRINSIC: $7.71fF + 3.7ff = \underline{11.41ff}$

- INTRINSIC:

$$C_{gs} + C_{gb} = \frac{2}{3} C'_{ox} \left(\frac{1+2\alpha}{1+\alpha^2}\right)\left(\frac{\sqrt{1+i_f} - 1}{\sqrt{1+i_f}}\right) + \frac{n-1}{n}\left(C'_{ox} - C_{gs} - C_{gd}\right)$$

C_{gd} → NEGLIGIBLE SINCE DEVICE IS ACTIVE

$$1 - \frac{n-1}{n} = \frac{n - n + 1}{n} = \frac{1}{n}$$

$$C_{gs} + C_{gb} \cong \frac{1}{n} C_{gs} + \frac{n-1}{n} C'_{ox}$$

$$i_f = 10 \Rightarrow \alpha \cong \frac{1}{\sqrt{11}} = 0.301$$

$$\frac{\sqrt{11} - 1}{\sqrt{11}} = 0.7$$

$$C_{gs} + C_{gb} \simeq \frac{1}{n} \times 0.211\, C'_{ox} + \frac{n-1}{n} C'_{ox}$$

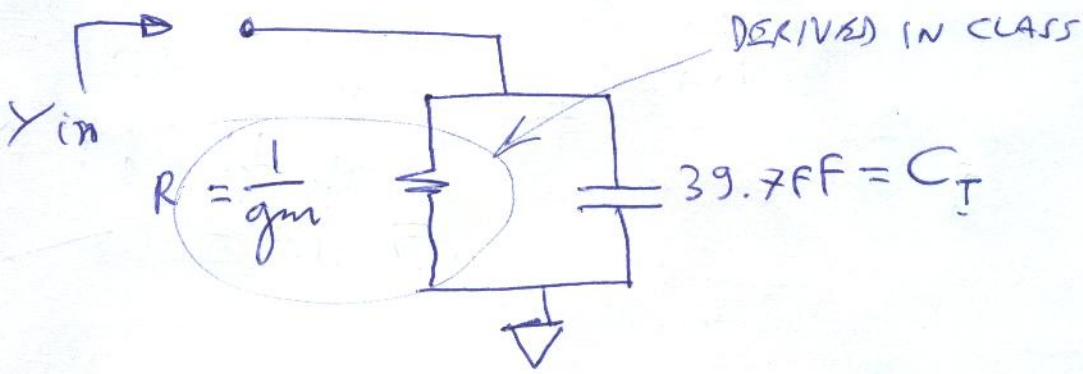
$$= 0.393\, C'_{ox} = 0.393 \times 80.74fF$$

$$= \underline{31.7fF}$$

INTRINSIC
∴ GATE CAPACITANCE IS DOMINANT

TOTAL CAPACITANCE TO GROUND = **50.8 fF**

c)



$$g_m = g_{mg} = \frac{2I_S}{nV_T}\left(\sqrt{1+if} - 1\right) = 0.188\ mS$$

$$Y_{in} = g_m + j\omega C_T$$

$$\boxed{Y_{in} = 0.188\ mS + j2\pi f \times 50.8\ fF}$$