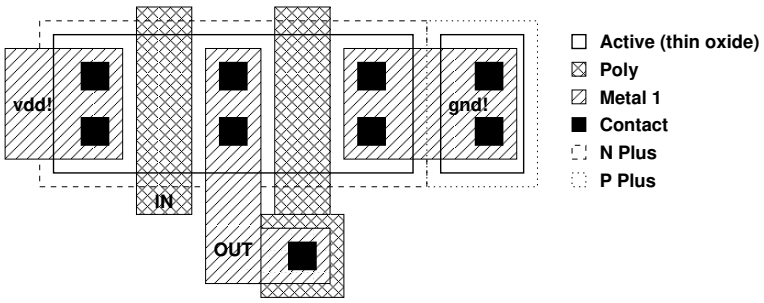
EELE 5131
Assignment 3 — Winter 2019

Problems

1. The following layout is for a process with p-type substrate. Draw an schematic diagram of the circuit in this layout. Use the provided node labels.



2. Using thin-oxide PMOS transistors (`pch` model), design a simple current mirror according to the following specifications:

   - Input current is 3 μA
   - Nominal output current is 2 μA
   - Supply voltage is 1.8 V
   - Maximum operating output voltage is 1.6 V
   - $\sigma(\Delta I_o/I_o)$ due to mismatch must be 2% or lower. Consider $A_{VT} = 4.1$ mVμm and $A_\beta = 0.03$ μm.
   - $\Delta I_o/I_o \leq 3\%$ for an output voltage change of 1 V.
   - Use unit transistors for improved matching. Try to minimize gate area.
   - Specify final design as follows: unit transistor dimensions and circuit diagram.

3. Perform the "6. Layout Creation" tutorial and create the layout for the current mirror designed in Problem 2. Define 3 connections (pins) for the layout: vdd!, iin, iout. Export your layout to stream format using the instructions in the tutorial page ("8. Brief instructions ...") and e-mail the layout to the instructor as an attachment.

4. A diode-connected thin-oxide NMOS transistor (`nch` model) is rectangular and has the following dimensions: $W = 10$ μm, $L = 1$ μm and the width of the drain and source regions is 0.48 μm. The transistor is biased such that $i_f = 10$ and the source and bulk are grounded.

   (a) Calculate I_D and V_G.

   (b) Calculate the extrinsic and intrinsic capacitances that contribute to the drain-ground capacitance. Which capacitance is the dominant component?

   (c) Calculate the input admittance seen from the drain node to ground as a function of frequency.