Transient Analysis of Nonlinear Circuits Based on Waves

Carlos Christoffersen

Abstract A new approach for transient analysis of nonlinear circuits is presented. The circuit equations are formulated as functions of incident and reflected waves at the device ports. Only one large matrix decomposition is necessary if time step is constant. The proposed method is parallelizable, allows straightforward inclusion of complex nonlinear device models and has better convergence properties compared to existing methods. Simulation results are provided to demonstrate the approach.

1 Introduction

Transient simulation of circuits using wave quantities has been previously proposed mainly in the framework of Wave Digital Filter (WDF) theory [1]. References [2–8] are some examples. WDF are discrete structures that mimic an analog reference circuit. The reference circuit is not required to be a filter and thus WDF theory can be applied to model any circuit. A good introduction of WDF concepts for the purpose of circuit simulation can be found in Reference [6]. The basic idea is to formulate equations in terms of wave quantities at the ports of each device. The network topology is represented by means of *adaptors*, which is the name for the scattering matrix representing port junctions. WDF preserve losslessness and passivity of the reference circuit, and are less sensitive to parameter quantization than discretizations based on voltage and current [7]. References [2, 3, 5, 7–10] show how nonlinear devices (both algebraic and dynamic) can be represented in terms of waves. In general it is not possible to avoid delay-free loops (DFLs) in circuits with more than one nonlinear port and thus some iterative method is required to solve the equations. References [9, 10] propose methods to eliminate DFLs created by multiple nonlinearities. These works basically propose to simultaneously compute

Carlos Christoffersen
Department of Electrical Engineering, Lakehead University, 955 Oliver Road, Thunder Bay, Ontario P7B 5E1, Canada e-mail: c.christoffersen@ieee.org

(or pre-compute) all possible reflections given all possible incident waves from all nonlinear ports. That kind of approach is useful only when the number of nonlinear ports is small. Reference [8] proposes a method to eliminate DFLs for circuits containing nonlinear inductors. This method relies on an estimation of the inductor current at each time step and can not be applied for algebraic nonlinearities. In Reference [6] WDF are used to simulate power electronic circuits with nonlinear devices treated as switches. A relaxation approach was proposed by Meerkötter *et al.* [3] to eliminate DFLs. This approach always converges for circuits that contain passive nonlinear devices that are also locally passive. Local passivity implies that the spectral radius of the device small-signal scattering parameter matrix is less than one (note transistors are not locally passive). Reference [4] further investigates this approach and shows that it is possible to cut DFLs and split the computation in independent blocks suitable for parallel processing without losing convergence.

The wave-based transient analysis approach presented in this work solves DFLs through an iterative procedure that has better convergence properties than previous works. Another advantage of the proposed approach is that allows easy inclusion of complex multiport nonlinear devices formulated in the Kirchhoff domain. Only one large (sparse) matrix decomposition is required for a given time step size. This paper is organized as follows: the formulation of the method and some of its properties are presented in Section 2, followed by simulation examples in Section 3. Conclusions and directions for further research are given in Section 4.

2 Proposed Method

In the following we will assume that all sources have some internal resistance and all remaining devices are passive as shown in Fig. 1. Let n be the total number of ports and m the number of nonlinear ports. For each port, we associate a characteristic impedance equal to Z_j. Since a time domain method is being considered, Z_j is pure real. The voltage and current at Port j can be expressed in terms of power waves as follows:

$$v_j = \sqrt{Z_j}(a_j + b_j) \tag{1}$$

$$i_j = \frac{a_j - b_j}{\sqrt{Z_j}}, \tag{2}$$

where a_j and b_j are the incident and reflected power waves at Port j as seen from the devices as shown in Fig. 1. The circuit topology defines the relationship between the vector of incident and reflected waves, **a** and **b**, respectively. Let **Q** and **B** be the full cut-set and loop-set matrices for a given tree in the circuit. The vectors of all port currents (**i**) and port voltages (**v**) satisfy

$$\mathbf{Qi} = \mathbf{0} \tag{3}$$

$$\mathbf{Bv} = \mathbf{0}. \tag{4}$$

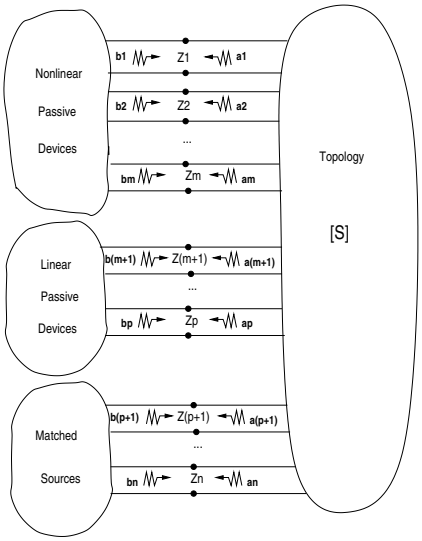

Fig. 1 Circuit partition. Linear and nonlinear devices are assumed to be passive and sources are assumed matched to the impedances of their respective ports. The interconnection (topology) is represented by a scattering parameter matrix.

Combining (1) and (2) with (3) and (4) the following system of n equations is obtained:

$$\begin{bmatrix} \mathbf{Q}\mathbf{D}^{-1} \\ \mathbf{B}\mathbf{D} \end{bmatrix} \mathbf{a} = \begin{bmatrix} \mathbf{Q}\mathbf{D}^{-1} \\ -\mathbf{B}\mathbf{D} \end{bmatrix} \mathbf{b}, \tag{5}$$

where $\mathbf{D}$ is a diagonal matrix that has the square root of the reference impedances ($\sqrt{Z_j}$) in its diagonal. Matrices $\mathbf{Q}$ and $\mathbf{B}$ are sparse and thus $\mathbf{a}$ can efficiently be obtained for large circuits if $\mathbf{b}$ is known. This equation defines the scattering matrix that represents the circuit topology,

$$\begin{bmatrix} \mathbf{a}_N \\ \mathbf{a}_L \\ \mathbf{a}_S \end{bmatrix} = \begin{bmatrix} \mathbf{S}_{11} & \mathbf{S}_{12} & \mathbf{S}_{13} \\ \mathbf{S}_{21} & \mathbf{S}_{22} & \mathbf{S}_{23} \\ \mathbf{S}_{31} & \mathbf{S}_{32} & \mathbf{S}_{33} \end{bmatrix} \begin{bmatrix} \mathbf{b}_N \\ \mathbf{b}_L \\ \mathbf{b}_S \end{bmatrix}, \tag{6}$$

where $\mathbf{a}_N$, $\mathbf{a}_L$ and $\mathbf{a}_S$ are the vectors of waves incident to nonlinear devices, linear devices and sources, respectively and $\mathbf{b}_N$, $\mathbf{b}_L$ and $\mathbf{b}_S$ are similarly defined for the reflected waves. The trapezoidal rule is used for time discretization as is usual in the WDF literature [6]. Reference resistances at sources and linear devices are chosen such that there are no DFL from the device back to the network [6]. Thus $\mathbf{b}_L$ is constant for one time step as all loops contain at least one delay.

2.1 Nonlinear Models

Nonlinear devices, both static and dynamic, will cause DFLs. Reflections are calculated in this work using Newton's method. For example, suppose the current in a

nonlinear device is given by a nonlinear function, $i(v_j)$. An error function, $e(a_j)$, is defined

$$e(a_j) = \sqrt{Z_j}\, i(\sqrt{Z_j}(a_j + b_j)) - a_j + b_j = 0\,. \tag{7}$$

This can easily be generalized for multi-port nonlinear devices, both static and dynamic. Newton iterations are performed independently for each nonlinear device and require a small Jacobian matrix factorization. One advantage of this approach is that it allows straightforward treatment of complex nonlinear models.

2.2 Iterative Method

Vector $\mathbf{b}_S$ is known since it is forced by the matched sources. The nonlinear equation to be solved is thus

$$\mathbf{b}_N = \mathbf{F}(\mathbf{S}_{11}\mathbf{b}_N + \mathbf{a}_0)\,, \tag{8}$$

with $\mathbf{a}_0 = \mathbf{S}_{12}\mathbf{b}_L + \mathbf{S}_{13}\mathbf{b}_S$ being constant for a given time instant and $\mathbf{F}$ is a nonlinear vector function that represents the contribution of nonlinear passive devices. The following iterative fixed-point scheme is proposed:

$$\mathbf{b}_N^{k+1} = (\mathbf{I} - \mathbf{K}^k)\mathbf{b}_N^k + \mathbf{K}^k\mathbf{F}(\mathbf{S}_{11}\mathbf{b}_N^k + \mathbf{a}_0)\,, \tag{9}$$

where the k superscript denotes the iteration number, $\mathbf{I}$ is an identity matrix and $\mathbf{K}^k$ is an $m \times m$ matrix that may be constant or updated at each iteration as described in the following subsection.

2.2.1 Convergence Analysis

Assume for now that $\mathbf{K}^k = \mathbf{I}$. In that case (9) is equivalent to just propagating reflections along the DFLs in the circuit (*i.e.*, plain relaxation). It can be shown that iterations converge to the desired solution if the spectral radius of $\mathbf{J}_F\mathbf{S}_{11}$ is less than one, where $\mathbf{J}_F$ is the Jacobian matrix of $\mathbf{F}$. This condition is satisfied if all nonlinear devices are locally passive (*e.g.*, diodes) and in this case convergence is global. Unfortunately convergence is not guaranteed if devices such as transistors are present in the circuit. Consider now a scalar (γ) between 0 and 1 and let

$$\mathbf{K}^k = \gamma\mathbf{I}\,. \tag{10}$$

Equation (9) becomes essentially equivalent to the formulation proposed in Reference [4]. A good selection of γ may improve convergence properties compared to plain relaxation but this modification is not enough to guarantee convergence in the presence of locally active devices.

Local convergence can be obtained by setting

$$\mathbf{K}^k = \left(\mathbf{I} - \mathbf{J}_F^k \mathbf{S}_{11}\right)^{-1}. \tag{11}$$

Equation (9) becomes then equivalent to Newton's method. Note that $\mathbf{J}_F$ is a block-diagonal matrix with each block being the small-signal scattering matrix for each nonlinear device. Although it is possible to re-order (5) and (9) in order to perform one sparse matrix decomposition per iteration, this is more expensive than the backward substitution of the relaxation approach.

One possibility to avoid the factorization of a large matrix at each iteration is to make $\mathbf{K}^k$ artificially sparse. If elements of $\mathbf{S}_{11}$ in (11) are set to zero to obtain the same block-diagonal pattern as in $\mathbf{J}_F$, the resulting $\mathbf{K}^k$ matrix is also block-diagonal. This requires explicit knowledge of $\mathbf{S}_{11}$ which in turn requires m backward substitutions of the decomposed matrix originating from (5), but this only need to be performed once. The resulting iterative scheme is known as Newton-Jacobi algorithm [11]. Local convergence is no longer guaranteed but it will be shown in Section 3 that this modification is an improvement over the relaxation approach.

2.2.2 Reflected Power Considerations

An interesting property of the pure relaxation approach ($\mathbf{K}^k = \mathbf{I}$) is that due to the nature of power waves iterations are guaranteed not to diverge to infinity, even if the initial guess is far from the solution. This is demonstrated as follows: The total reflected power at each iteration is given by $|\mathbf{b}_N^{k+1}|^2$, where the bars denote the Euclidean Norm, and is bounded by

$$|\mathbf{b}_N^{k+1}|^2 < P_{\max} + L|\mathbf{S}_{11}\mathbf{b}_N^k + \mathbf{a}_0|^2, \tag{12}$$

here L is a scalar less than one (since nonlinear devices are passive) and $P_{\max}$ is the maximum power that can be sent from the nonlinear devices to the network during one time step and depends on the total energy stored in nonlinear capacitors and inductors. If the upper bound is propagated from the first iteration the following result is obtained:

$$\lim_{k\to\infty} |\mathbf{b}_N^{k+1}|^2 < \frac{1}{1-L}\left(P_{\max} + L|\mathbf{a}_0|^2\right). \tag{13}$$

An upper bound can also be found if $\mathbf{K}^k$ is chosen as in (10). This property can be extended to the Newton-Jacobi approach if $\mathbf{K}^k$ is chosen as follows:

$$\mathbf{K}^k = \alpha\gamma\mathbf{I} + (1-\alpha)\mathbf{K}_{\mathrm{NJ}}^k, \tag{14}$$

where $\mathbf{K}_{\mathrm{NJ}}^k$ is the block diagonal matrix used for the Newton-Jacobi approach and α is the lowest scalar between 0 and 1 such that $\mathbf{b}_N^{k+1}$ satisfies (12). For circuits with locally passive nonlinear devices this choice tends to provide both global convergence when initial guess is far from the solution and faster convergence rate near the solution as α becomes 0.

In summary, iterations are performed according to (9) using $\mathbf{K}^k$ as defined in (14). Thus the proposed method is an hybrid between relaxation and Newton-Jacobi. Steffensen [12] updates,

$$b_j^{k+1} = b_j^{k-2} + \frac{(b_j^{k-1} - b_j^{k-2})^2}{b_j^k - 2b_j^{k-1} + b_j^{k-2}} \,, \tag{15}$$

are ocasionally used along with regular iterations to accelerate convergence. All calculations in (9) and (15) can be performed locally for each nonlinear device and thus could be computed in parallel. The only communication between processors at each iteration is to evaluate the product $\mathbf{S}_{11}\mathbf{b}_N^k$ which requires the reflections from all nonlinear devices.

3 Numerical Example

The circuit shown in Fig. 2 contains both static and dynamic nonlinearities included in the diode model. Since diodes are locally passive, convergence is guaranteed in this case. The circuit parameters are: $C = 4\ \mu$F, $R_S = 50\ \Omega$, $R_L = 5$ kΩ. The source is sinusoidal with a peak of 3 V (later increased to 200 V) and a frequency of 500 Hz. The diode parameters are $I_S = 1$ fA, N = 1, $C_j = 100$ nF, $M_j = 0.5$, $V_j = 1$ V and $F_C = 0.5$. Tolerance was set to 10^{-8}. A transient simulation with a duration of 8 ms and a time step equal to 50 μs was performed. Figure 2 also shows a comparison of simulation results obtained with the proposed algorithm and Spice.

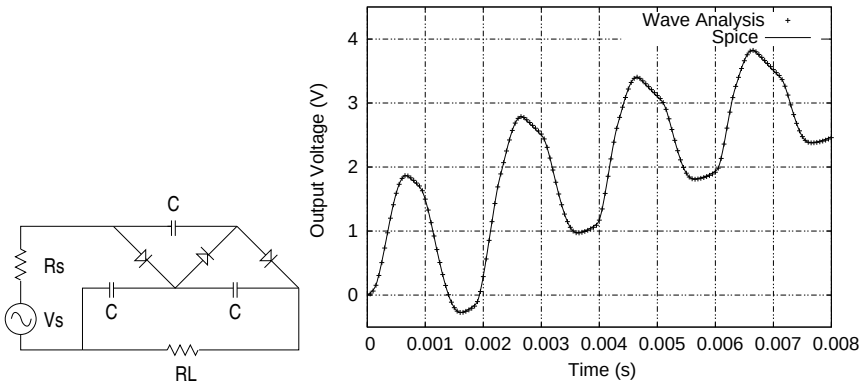

Fig. 2 Nonlinear circuit and comparison of simulation results at load resistor with 3 V input

Table 1 summarizes the results for different input voltages, reference impedances at the diode ports. The number of time steps is the same for all simulations. The last column indicates how many iterations with $\alpha \neq 0$ (*i.e.*, limited reflected power) were performed. The first three rows show the results when the full Jacobian ma-

Table 1 Summary of simulation results

Input (V)	Ref. Impedance (Ω)	Steffensen U.	Total Iterations	Reflected Power Limit
3	50	disabled	[a]763	56
3	500	disabled	[a]806	15
200	500	disabled	[a]1950	1141
3	50	87	[b]4897	0
3	500	271	[b]3591	0
200	500	disabled	[b]42075	0
200	500	250	[b]13836	0
3	50	disabled	5225	1
3	50	62	4412	1
3	500	disabled	2518	4
3	500	27	2483	4
200	500	disabled	10234	1234
200	500	138	6852	953

[a] Regular Newton method + Power limit
[b] Pure relaxation

trix is used instead of a block-diagonal matrix. The choice of reference impedance does not significantly affect the convergence rate for that case, but this is not so when pure relaxation or the modified Newton-Jacobi method is used as seen in the remaining rows of the table. The most nonlinear cases (200 V input) show that both Steffensen updates and reflected power limitation are frequently used. Selective Steffensen updates improve convergence in all cases. It should be noted that sometimes the reflected power limitation reduces somewhat the convergence rate. However even when that happens the proposed approach converges faster than plain relaxation.

4 Conclusions and Discussion

The proposed method has the good numerical properties associated with the WDF approach and allows the inclusion of complex nonlinear device models. Equation (9) introduces a cause-effect relation in the power delivered to nonlinear devices that is not apparent in more classical approaches. That formulation along with selective Steffensen's updates, the treatment of nonlinear device models and the approach to prevent numerical divergence with Newton-Jacobi iterations are novel in this work. An admittedly simple nonlinear circuit was simulated to illustrate the performance of the proposed method. It was shown that the combination of the techniques proposed here improves the convergence rate compared with plain relaxation. As expected, Newton-Jacobi iterations do not converge as fast as regular Newton iterations. Newton-Jacobi could be faster however for large circuits as the cost of iterations does not grow as much with the circuit size. The performance of the proposed method with large scale circuits has yet to be evaluated.

Circuits with locally active devices (*e.g.*, transistors) can be handled by this method but then convergence is no longer guaranteed. Work in progress indicates that with some modifications it is possible to guarantee (at least local) convergence in that case. The analysis presented here is for fixed time step, but variable time step could be handled without additional matrix decompositions by considering variable reflections from linear devices, *i.e.* $\mathbf{b}_L$ changes with each iteration. There is an associated computational cost with this modification, but the main features of the method remain intact. Another important issue is the optimum selection of reference impedances at nonlinear device ports. This selection may have to be adaptive since the optimum values are dependent on the circuit state. Further research will also include the application of the ideas presented here for other types of circuit analysis such as Harmonic Balance, or Envelope Following Transient.

Acknowledgements This work was funded by the Natural Sciences and Engineering Research Council of Canada (NSERC).

References

1. Fettweis, A.: Wave Digital Filters: Theory and Practice. IEEE Proceedings, **74**, 270–327 (1986)
2. Meerkötter, K. and Scholz, R.: Digital simulation of nonlinear circuits by wave digital filter principles. In: Proc. IEEE ISCAS '89, pp. 720–723. Portland, May 8–11 (1989)
3. Meerkötter, Felderhoff, T.: Simulation of nonlinear transmission lines by wave digital filter principles. In: Proc. IEEE ISCAS '92, pp. 875–879. San Diego, May 3–6 (1992)
4. Felderhoff, T.: Jacobi's method for massive parallel wave digital filter algorithm. In: Proc. of the IEEE Conference on Acoustics, Speech and Signal Processing, pp. 1621–1624. Atlanta, May 7–10 (1996)
5. Felderhoff T.: A new wave description for nonlinear elements. In: Proc. IEEE ISCAS '96, pp. 221–224. Atlanta, May 12–15 (1996)
6. Fiedler, A., Grotstollen, H.: Simulation of power electronic circuits with principles used in wave digital filters. IEEE Trans. on Indutry Applications, **33**, 49–57. (1997)
7. Sarti, A., De Poli, G.: Towards nonlinear wave digital filters, IEEE Trans. on Signal Processing, **47**, 1654–1668. (1999)
8. Fränken, D.: Wave digital simulation of electrical networks containing nonlinear dynamical elements — a new approach. In: Proc. IEEE ISCAS 2000, pp. 535–538. Geneva, May 28–31 (2000)
9. Petrausch, S., Rabenstein, R.: Wave digital filters with multiple nonlinearities. In: Proc. of the 12th European Signal Processing Conf. (2004) http://www-nt.e-technik.uni-erlangen.de/LMS/publications/web/lnt2004_22.pdf. Cited 8 Sept. 2008
10. Borin, G., De Poli, G., Rocchesso, D.: Elimination of delay-free loops in discrete-time models of nonlinear acoustic systems. IEEE Trans. on Speech And Audio Processing, **8**, 597–605. (2000)
11. Bahi, J. M., Contassot-Vivier, S., Couturier, R.: Parallel Iterative Algorithms, Chapman & Hall / CRC, Boca Raton London New York (2008)
12. Burden, R., Faires, J.: Numerical Analysis, Fifth Edition, Prindle, Weber & Schmidt, Boston (1993)