Transient Analysis of Nonlinear Circuits Based on Waves

Carlos Christoffersen¹

Department of Electrical Engineering, Lakehead University, 955 Oliver Road, Thunder Bay, Ontario P7B 5E1, Canada c.christoffersen@ieee.org.

Summary. A new approach for transient analysis of nonlinear circuits is presented. The circuit equations are formulated as functions of waves in fictitious transmission lines. The waves are calculated following a procedure that resembles the actual signal propagation in a circuit and is fully parallelizable. A strongly nonlinear circuit is used as a case study.

1 Introduction

Circuit-level simulation of complex systems is a challenging task in terms of memory and CPU time. It is thus of great interest to find more efficient methods for circuit-level simulation. At the core of nonlinear circuit analysis is the solution of a system of nonlinear algebraic equations. Solving this system of equations using Newton method requires the decomposition of a large (normally sparse) matrix for each iteration. This matrix is particularly large in the case of harmonic balance (HB) or techniques based on multiple time dimensions [1].

This paper presents a transient analysis approach that requires only one matrix decomposition for a given time step size. This approach was inspired in the multiple reflections technique [2] and wave digital simulation of circuits [3,4]. Wave digital filters [5] were developed to replace analog filters with a digital structure. Several methods have been proposed for transient simulation using waves but they have limitations handling nonlinearities or do not scale well with the size of the circuit. Felderhoff [3] proposed a convergent relaxation method that can treat several nonlinear devices and is easily parallelizable. The method proposed in this paper is also parallelizable and can handle arbitrary static and dynamic nonlinearities.

2 Formulation

Assume that the total number of ports of all devices in a given circuit is equal to n. For each port, we associate a reference impedance Z_j . The voltage and current at Port j can be expressed as

$$v_j = v_j^+ + v_j^- (1)$$

$$i_j = \frac{v_j^+ - v_j^-}{Z_j},$$
 (2)

where v_j^+ and v_j^- are the incident and reflected waves at Port j as seen from the devices as shown in Fig. 1. The circuit topology defines the rela-

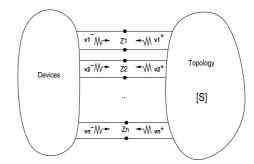


Fig. 1. Circuit partition

tionship between the vector of incident and reflected waves, \mathbf{v}^+ and \mathbf{v}^- , respectively. Let \mathbf{Q} and \mathbf{B} be the full cut-set and loop-set matrices for a given tree in the circuit. The vectors of all port currents (i) and port voltages (v) satisfy

$$\mathbf{Qi} = \mathbf{0} \tag{3}$$

$$\mathbf{B}\mathbf{v} = \mathbf{0}. \tag{4}$$

Combining (1) and (2) with (3) and (4) the following equation is obtained:

$$\begin{bmatrix} \mathbf{QG} \\ -\mathbf{B} \end{bmatrix} \mathbf{v}^+ = \begin{bmatrix} \mathbf{QG} \\ \mathbf{B} \end{bmatrix} \mathbf{v}^- \,,$$

where **G** is a diagonal matrix that has the reciprocal of the reference impedaces (Z_j) in its diagonal. Matrices **Q**, **G** and **B** are sparse and thus \mathbf{v}^+ can efficiently be obtained for large circuits.

The reference impedance at sources and linear devices can be chosen such that there are no reflections from the device back to the network [4]. Nonlinear devices will cause reflections. In this paper it is proposed to calculate these reflections using Newton's method. For example, suppose the current in a nonlinear device is given by

$$i_i = f(v_i)$$
,

with f() a nonlinear function. An error function is defined as follows:

$$F(v_i^+) = Z_j f(v_i^+ + v_i^-) - v_i^+ + v_i^- = 0.$$

This can easily be generalized for multi-port nonlinear devices, both static and dynamic. Moreover, the same idea can be applied to a complete subcircuit.

Using this formulation, only one large matrix decomposition is necessary for the complete simulation. This decomposition could eventually be eliminated if an automatic way to decompose the topology in adaptors is developed. The computation performed at each iteration is completely parallelizable: propagation of waves through the topology is essentially a matrix-vector product and the Newton method for each device is independent of the rest of the circuit. This iterative process resembles the actual propagation of signals in a physical circuit.

3 Case Study

The circuit shown in Fig. 2 was simulated to test the approach proposed in this paper. The circuit parameters are: $C=4~\mu\mathrm{F},~R_S=50~\Omega,$ $R_L=5~\mathrm{k}\Omega.$ The source is sinusoidal with a peak of 3 V and a frequency of 500 Hz. The diode parameters are $I_S=1~\mathrm{fA},~N=1,~C_j=100~\mathrm{nF},$ $M_j=0.5,~V_j=1~\mathrm{V}$ and $F_C=0.5$. The reference impedances were chosen to avoid reflections where possible and a value of 50 Ω was used for the diode ports. A transient simulation with a du-

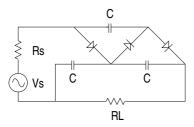


Fig. 2. Nonlinear circuit

ration of 8 ms and a time step equal to 50 μ s was performed. The simulation results are compared with a Spice simulation in Fig. 3.

The convergence of this method as described here is linear, but it can be made superlinear using Steffensen-like updates. An average of 30 iterations per sample point were necessary to achieve a tolerance of 10^{-8} . The number of iterations was at least 11 and at most 42 for each sample point.

Several issues must still be addressed. The most important is a rigorous convergence analysis. Another issue is that the choice of reference

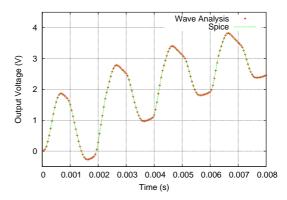


Fig. 3. Comparison of voltages at load resistor

impedance in each nonlinear port affects the convergence rate, but currently there is no method to predict the optimum value.

The Spice simulation is significantly faster in this example, but the proposed method was not optimized for speed. Many improvements are still possible to reduce the computational cost of each iteration. If a comparable performance can be achieved for small circuits, then due to its parallel nature the proposed method may become more efficient for very large circuits or when applied to analyses where several samples/harmonics are calculated at once such as in HB or techniques based on multiple time dimensions [1].

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