Transient Simulation Based on State Variables and Waves

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Abstract

This paper reports a new method for transient analysis of nonlinear circuits based on nonlinear device state variables and waves at their ports. The method is based on relaxation and thus does not require large matrix decompositions if time step is constant. The use of waves results in guaranteed convergence for any linear passive circuit and some types of nonlinear circuits. Additionally, the formulation using waves ensures that nonlinear devices are always excited with a physically meaningful input, *i.e.*, the amount of power transmitted to nonlinear devices is bounded. The method was implemented in the *f*REEDA™ circuit simulator. The formulation, its properties and a convergence analysis of the proposed method are presented first, followed by case studies.

keywords: Transient Analysis, Waves, Scattering Matrix, Wave Digital Filters, Iterated Timing Analysis, State Variables, Fixed-point Iteration, Minimum Polynomial Extrapolation.

1 Introduction

Circuit-level simulation of large circuits is a challenging task in terms of memory and CPU time. Nonlinear circuit elements add more complexity due to the need of solving a system of nonlinear algebraic equations. It is thus of great interest to find efficient simulation methods. One advantage of transient analysis compared to other techniques is its capability to handle very strong nonlinearities of large circuits. The fact that small time steps can be used in time-domain integration makes this analysis robust [1]. Thus transient analysis is a promising start to evaluate the ideas presented here. The transient analysis formulation presented in this work is based on fixed-point iterations of waves at the ports of nonlinear devices. The greatest advantage of this approach compared to the traditional fixed-point iteration approaches using voltages and currents is that the power delivered to nonlinear devices at any iteration is bounded [2]. There is very little work in the literature exploring this idea.

Previously waves have been used for transient simulation in the context of wave digital filters (WDF) [3]. WDF are discrete structures that mimic an analog reference circuit. The reference circuit is not required to be a filter and thus WDF theory can be applied to model any circuit. Equations are formulated

in terms of wave quantities at the ports of each element in a circuit. The interconnection of elements is represented by means of *adaptors* [4]. Nonlinear devices (both algebraic and dynamic) can be modeled in terms of waves [5–11]. For circuits with more than one nonlinear device port, delay-free loops (DFLs) in the wave paths are likely to be formed [6]. DFLs prevent the direct computation of waves in the circuit. Some approaches exist [10,11] to eliminate DFLs created by multiple nonlinearities. Basically all nonlinear devices and some interconnections are lumped in a sub-circuit and the reflections from its ports are pre-computed given all possible combinations of incident waves. That kind of approach is useful only when the number of nonlinear devices is small. Reference [8] proposes a method to eliminate DFLs focused on circuits with nonlinear inductors only. Fiedler *et al.* in [4] employed WDF theory applied to the simulation of power electronic circuits. Nonlinear devices are treated as switches in this work.

Traditional transient analysis formulations based on Newton's method require the solution of a set of simultaneous linear equations. Matrix decomposition of a large Jacobian matrix is required at each Newton iteration. Fixed-point (or relaxation) methods exploit the latency of the circuit by decoupling it into smaller pieces and solving each piece independently [12]. Thus a matrix decomposition per iteration is not required in these methods and they are more suitable to be implemented in parallel computer systems to perform the numerical calculations concurrently. Different relaxation methods have been previously proposed for circuit simulation [13–15,21], among those Iterated Timing Analysis (ITA) and Waveform Relaxation (WR) are explored most. In ITA, relaxation process is continued until convergence is achieved at each time point [13]. On the other hand, WR is based on solving the decoupled sub-circuits independently over an interval of time rather than for a single time point [12]. Some considerable research works have been performed for the parallel implementation of both WR [22–24] and ITA [25, 26]. More recently a variant of waveform relaxation (transverse waveform relaxation) have succesfully been applied to the parallel simulation of coupled interconnects [16, 17]. Improved convergence of WR for linear tightly coupled systems such as longitudinal partitioning of transmission lines has also been recently reported [18, 19]. In order to obtain convergence for tightly coupled circuits, it is not enough to exchange just voltages between the different circuit blocks, a combination of voltages and currents (or equivalent) is needed [18–20]. These results suggest that a relaxation approach based on waves, which can be seen as a combination of voltage and current in a port, may have good convergence properties.

Circuit simulation using relaxation in the WDF context was explored in References [6] and [2]. The approach in [2] allows nonlinear devices to be modeled using voltages and currents, and thus it is more suitable for implementation in a circuit simulator. In this paper the method proposed in [2] is further developed with parameterized nonlinear device models, implemented in the *f*REEDA™ [27] simulator and tested with a wider variety of circuits.

The main purpose of this work is to determine the feasibility of the relaxation approach based on waves applied to practical circuits and to further

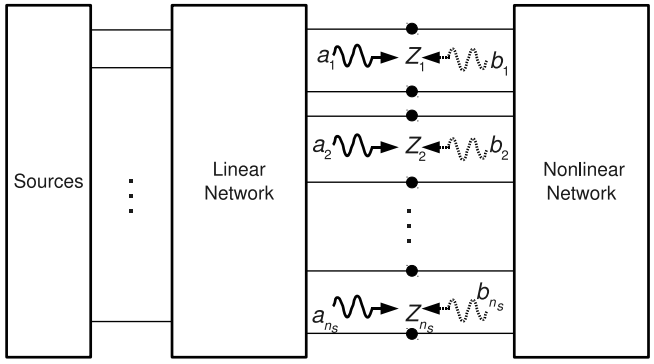

Figure 1: Network partition

study its convergence properties. A derivation of the relevant equations and the iteration scheme is presented in Section 2. Section 3 analyzes convergence properties. It is shown that the proposed approach is globally convergent for linear passive circuits and at least locally convergent for some types of nonlinear circuits. The effects of vector extrapolation methods to accelerate convergence are investigated here for the first time. Simulation results for several circuits are presented and discussed in Section 4.

2 Formulation

2.1 State-Variable Formulation

Equations are formulated following the state-variable approach [29] used in *f*REEDA™. The circuit is partitioned in sources, linear and nonlinear parts (Fig. 1). For each nonlinear element ports are defined with one terminal taken as the reference. The linear network is assumed to be passive.

A circuit containing nonlinear elements is described by the time domain MNA equation as follows:

$$\mathbf{M}\mathbf{u}(t) + \mathbf{C}\frac{d\mathbf{u}(t)}{dt} + \int_0^t \mathbf{Y}(\tau)\mathbf{u}(t-\tau)d\tau + \mathbf{S}_{NL}(t) = \mathbf{S}_f(t), \tag{1}$$

where $\mathbf{M}$, $\mathbf{C}$ and $\mathbf{Y}(t)$ are $n_u \times n_u$ matrices and $\mathbf{u}(t)$ is a vector with n_u elements consisting of nodal voltages plus additional variables. The $\mathbf{M}$ matrix contains all conductors and frequency-independent MNAM stamps arising in the formulation, $\mathbf{C}$ consists of capacitor and inductor values and other values that are associated with dynamic elements and $\mathbf{Y}(t)$ is a matrix containing the impulse response of all distributed linear networks. For causal networks $\mathbf{Y}(t) = 0$ for

$t < 0$. The $\mathbf{S}_f(t)$ vector contains the independent sources contributions and $\mathbf{S}_{NL}(t)$ contains the currents of the nonlinear devices.

The nonlinear subnetwork is described by the following parametric equations [31]:

$$\mathbf{v}_{NL}(t) = \mathbf{v}\left(\mathbf{x}(t), \frac{d\mathbf{x}}{dt}, \ldots, \frac{d^m\mathbf{x}}{dt^m}, \mathbf{x}_D(t)\right) \quad (2)$$

$$\mathbf{i}_{NL}(t) = \mathbf{i}\left(\mathbf{x}(t), \frac{d\mathbf{x}}{dt}, \ldots, \frac{d^m\mathbf{x}}{dt^m}, \mathbf{x}_D(t)\right) \quad (3)$$

where $\mathbf{v}_{NL}(t)$, $\mathbf{i}_{NL}(t)$ are vectors of voltages and currents at the ports of the nonlinear network, $\mathbf{x}(t)$ is a vector of state variables and $\mathbf{x}_D(t)$ is a vector of time-delayed state variables, *i.e.*, $(x_D)_i(t) = x_i(t - \tau_i)$. All vectors in Eqs. (2) and (3) have the same size equal to the number of ports of the nonlinear network (n_s). We will adopt the passive convention for voltages and currents at the nonlinear device ports.

The connectivity information between the linear and nonlinear subnetwork is given by a sparse incidence matrix ($\mathbf{T}$) of size $n_u \times n_s$:

$$\mathbf{v}_{NL}(t) = \mathbf{T}\mathbf{u}(t)\ , \quad (4)$$

$$\mathbf{S}_{NL}(t) = \mathbf{T}^T\mathbf{i}_{NL}(t)\ . \quad (5)$$

For simplicity, in this derivation $d\mathbf{u}(t)/dt$ will be approximated using the Backward Euler (BE) rule,

$$\frac{d\mathbf{u}(t)}{dt} \approx \frac{1}{h}(\mathbf{u}_n - \mathbf{u}_{n-1})\ ,$$

with h being the time step size, assumed to be constant, n the time step number and $\mathbf{u}_n = \mathbf{u}(t_n)$. This derivation is very similar [29] when using other integration methods such as the Trapezoidal method. The state variable vector ($\mathbf{x}$) is discretized in a similar way.

Applying the BE method and discrete convolution, Eqs. (1) and (5) are combined:

$$\mathbf{A}\mathbf{u}_n = \mathbf{S}_{f,n} - \mathbf{T}^T\mathbf{i}_{NL}(\mathbf{x}_n, \mathbf{x}_{n-1}, \ldots) + \frac{1}{h}\mathbf{C}\mathbf{u}_{n-1} - \sum_{l=1}^{\infty}\mathbf{Y}_l\mathbf{u}_{n-l} \quad (6)$$

$$\mathbf{A} = \mathbf{G} + \frac{1}{h}\mathbf{C} + \mathbf{Y}_0\ , \quad (7)$$

where $\mathbf{Y}_l = \mathbf{Y}(t_l)$ and $\mathbf{Y}_0 = \mathbf{Y}(0)$. Solving for $\mathbf{u}_n$ in Eq. (6) and combining with Eq. (4) the following error function is obtained:

$$\mathbf{s}_{sv,n} - \mathbf{M}_{sv}\mathbf{i}_{NL}(\mathbf{x}_n, \mathbf{x}_{n-1}, \ldots) - \mathbf{v}_{NL}(\mathbf{x}_n, \mathbf{x}_{n-1}, \ldots) = 0\ , \quad (8)$$

with

$$\mathbf{s}_{sv,n} = \mathbf{T}\mathbf{A}^{-1}\left(\mathbf{S}_{f,n} + \frac{1}{h}\mathbf{C}\mathbf{u}_{n-1} - \sum_{l=1}^{\infty}Y_l\mathbf{u}_{n-l}\right)$$

$$\mathbf{M}_{sv} = \mathbf{T}\mathbf{A}^{-1}\mathbf{T}^T\ .$$

Note that $\mathbf{M}_{sv}$ is constant and $\mathbf{s}_{sv,n}$ depends only on quantities that are known at the nth time step. The size of the algebraic system of nonlinear equations (8) is $n_s \times n_s$. For microwave circuits n_s is often much smaller than n_u.

2.2 Formulation in Terms of Waves

For each nonlinear port, we now adopt an arbitrary reference resistance, R_j with j the port number. In this work, the incident and reflected waves at Port j (a_j and b_j, respectively) are defined as follows,

$$a_j = \frac{v_j + R_j i_j}{2\sqrt{R_j}} \ , \ b_j = \frac{v_j - R_j i_j}{2\sqrt{R_j}} \ ,$$

where v_j and i_j are the instantaneous values of the voltage and current at the port. Note that the instantaneous power flow to the nonlinear device in Port j is equal to $(a^2 - b^2)$. These waves are known as *power waves* [3] in the WDF literature and they are a special case of Kurokawa's [32] power waves if R_j is thought as the resistance of a generator driving the nonlinear port. These waves can also be thought as travelling waves in imaginary zero-length lossless transmission lines with a characteristic impedance equal to R_j, as shown in Fig. 1.

The voltage and current at Port j can be expressed as

$$\begin{aligned} v_j &= \sqrt{R_j}(a_j + b_j) \ , \\ i_j &= \frac{(a_j - b_j)}{\sqrt{R_j}} \ . \end{aligned}$$

Thus voltage and current vectors corresponding to all nonlinear device ports are related to the wave vectors ($\mathbf{a}$ and $\mathbf{b}$) as follows:

$$\mathbf{v}_{NL} = \mathbf{D}(\mathbf{a} + \mathbf{b}) \ , \tag{9}$$

$$\mathbf{i}_{NL} = \mathbf{D}^{-1}(\mathbf{a} - \mathbf{b}) \ , \tag{10}$$

where $\mathbf{D}$ is a diagonal matrix with the square root of reference port resistances.

The proposed relaxation method is based on propagating reflections of waves between the linear and nonlinear subnetworks. Assume an initial vector of reflected waves ($\mathbf{b}_n^k$) is known, where k denotes the iteration number. The corresponding waves sent by the linear network ($\mathbf{a}_n^{k+1}$) can be calculated by replacing Eqs. (9) and (10) in Eq. (8),

$$\mathbf{a}_n^{k+1} = \mathbf{S}\mathbf{b}_n^k + \mathbf{a}_{0,n} \ , \tag{11}$$

with

$$\mathbf{S} = [\mathbf{M}_{sv}\mathbf{D}^{-1} + \mathbf{D}]^{-1}[\mathbf{M}_{sv}\mathbf{D}^{-1} - \mathbf{D}] \ , \tag{12}$$

$$\mathbf{a}_{0,n} = -[\mathbf{M}_{sv}\mathbf{D}^{-1} + \mathbf{D}]^{-1}\mathbf{s}_{sv,n} \ , \tag{13}$$

here, $\mathbf{S}$ is the scattering matrix of the linear network and $\mathbf{a}_{0,n}$ is the source contribution to the incident waves. If $\mathbf{M}_{sv}$ exists then the inverse of $[\mathbf{M}_{sv}\mathbf{D}^{-1} + \mathbf{D}]$ must also exist.

Wave equations for the nonlinear device side are derived next. Under certain conditions [5,7,9], the effect of nonlinear devices can be expressed as a nonlinear vector function $\mathbf{F}(\ )$,

$$\mathbf{b}_n^{k+1} = \mathbf{F}(\mathbf{a}_n^{k+1}) \ . \tag{14}$$

Equation (14) in general is not explicitly available in circuit simulators. The approach adopted here is to use Newton's method at the nonlinear device level to solve for $\mathbf{b}_n^{k+1}$. Rearranging Eqs. (9) and (10) we obtain the $\mathbf{F}_v(\ )$ and $\mathbf{F}_i(\ )$ error functions:

$$\mathbf{F}_v(\mathbf{x}_n^{k+1}, \mathbf{b}_n^{k+1}) = \mathbf{D}^{-1}\mathbf{v}_{NL}(\mathbf{x}_n^{k+1}) - \mathbf{a}_n^{k+1} - \mathbf{b}_n^{k+1} \ , \tag{15}$$

$$\mathbf{F}_i(\mathbf{x}_n^{k+1}, \mathbf{b}_n^{k+1}) = \mathbf{D}\mathbf{i}_{NL}(\mathbf{x}_n^{k+1}) - \mathbf{a}_n^{k+1} + \mathbf{b}_n^{k+1} \ , \tag{16}$$

which must be equal to zero. The number of equations and unknowns is $2n_s$. The unknowns are vectors $\mathbf{b}_n^{k+1}$ and $\mathbf{x}_n^{k+1}$ as the vector of incident waves, $\mathbf{a}_n^{k+1}$ is known from Eq. (11). Note that this system of equations is decoupled for each nonlinear device, thus the Jacobian matrices arising from it are block-diagonal with small diagonal blocks, typically no more than 6×6 elements. The good numerical properties given by the parametric formulation of the nonlinear device equations [29] are retained (at the expense of having to solve for $\mathbf{x}_n^{k+1}$). The updates from each Newton iteration are calculated as follows

$$\Delta\mathbf{x} = [\mathbf{D}\mathbf{J}_I + \mathbf{D}^{-1}\mathbf{J}_V]^{-1}(-\mathbf{F}_i - \mathbf{F}_v) \ ,$$

$$\Delta\mathbf{b} = -\mathbf{F}_i - \mathbf{D}\mathbf{J}_I\Delta\mathbf{x} \ ,$$

Here $\mathbf{J}_I$ and $\mathbf{J}_V$ are the block-diagonal Jacobian Matrices of $\mathbf{v}_{NL}$ and $\mathbf{i}_{NL}$, respectively, which are explicitly available in *f*REEDA™, $\Delta\mathbf{x}$ and $\Delta\mathbf{b}$ are the updates of state variables and reflected waves at each Newton iteration. Most of the time only a few iterations (often only one) are required to reach an acceptable tolerance, as it is shown in Section 4.

The fixed-point scheme is summarized by combining Eqs. (14) and (11):

$$\mathbf{b}_n^{k+1} = \mathbf{F}(\mathbf{S}\mathbf{b}_n^k + \mathbf{a}_{0,n}) \ . \tag{17}$$

Note that $\mathbf{x}$ is only required at the nonlinear device level (Equations (15) and (16)) and is not required in the main loop (Eq. (17)).

3 Convergence Analysis

3.1 Bound on Wave Power

Although the formulation is different, Eq. (17) has the same form as Eq. (6) in Ref. [2]. The total reflected power at each iteration is given by $|\mathbf{b}_n^{k+1}|^2$, where the bars denote the Euclidean Norm, and is bounded by [2]

$$|\mathbf{b}_n^{k+1}|^2 < P_{max} + L|\mathbf{S}\mathbf{b}_n^k + \mathbf{a}_{0,n}|^2 \tag{18}$$

where L is a scalar, $0 < L < 1$ for passive nonlinear devices and P_{max} is a bound on the maximum average power that can be delivered from the nonlinear devices to the linear network during one time step and is given by $P_{max} = E_A/h$, where E_A is the total energy stored in nonlinear capacitors and inductors and h is the time step size. If this upper bound is propagated from the first iteration, it follows that

$$\lim_{k\to\infty} |\mathbf{b}_n^{k+1}|^2 < \frac{1}{1-L}(P_{max} + L|\mathbf{a}_{0,n}|^2) \; . \tag{19}$$

This property, which is a consequence of iterating waves, is useful because it ensures that iterations can never diverge to infinity and device models always have a physically meaningful excitation. If iterations are not convergent, steady-state oscillations in the error function are observed.

3.2 Local Convergence Analysis

Conditions for local convergence will be derived in the following. By performing a Taylor expansion around the solution of Eq. (17) (assumed here to be $\mathbf{b}_s$) and discarding higher-order terms, the following equation is obtained:

$$\mathbf{b}_n \approx \mathbf{b}_s + \mathbf{J}_f \mathbf{S} \left(\mathbf{b}_n - \mathbf{b}_s\right) \; , \tag{20}$$

where $\mathbf{J}_f$ is the Jacobian matrix of $\mathbf{F}(\;)$ in Eq. (17) and represents the small-signal scattering matrix of the nonlinear network. $\mathbf{J}_f$ is a block-diagonal matrix since $\mathbf{J}_I$ and $\mathbf{J}_V$ are block-diagonal. Assume that iterations are started at $\mathbf{b}_s + \xi_0$, with ξ_0 being an initial perturbation or error vector. Then the error at iteration $k+1$ (ξ_{k+1}) is given by

$$\xi_{k+1} \quad = \quad \mathbf{J}_f \mathbf{S} \xi_k \; , \tag{21}$$

The square of the 2-norm of ξ_{k+1} is then

$$|\xi_{k+1}|^2 = \xi_k^T \; [\mathbf{S}^T \mathbf{J}_f^T \mathbf{J}_f \mathbf{S}] \; \xi_k \; ,$$

where $\mathbf{J}_f^T$ denotes the transpose of $\mathbf{J}_f$. One sufficient condition for local convergence is that $\mathbf{J}_f\mathbf{S}$ corresponds to a passive network. In that case, the spectral radius [33] of $[\mathbf{S}^T\mathbf{J}_f^T\mathbf{J}_f\mathbf{S}]$ is less than one and $[\mathbf{I}-\mathbf{S}^T\mathbf{J}_f^T\mathbf{J}_f\mathbf{S}]$ is a positive semidefinite matrix [36] ($\mathbf{I}$ is the corresponding identity matrix). Thus $|\xi_{k+1}|^2$ decreases with k and iterations converge to the solution. $\mathbf{S}$ corresponds to a passive network, thus the proposed approach is always convergent for any circuit where nonlinear devices are locally passive (as defined in [34]). Rectifying diodes are locally passive. Unfortunately transistors may not be locally passive depending on the biasing point. Note that it is straightforward to extend this analysis for linear passive circuits. In that case convergence is guaranteed and global.

It is interesting to note that this convergence analysis is also valid for other circuit partitions. For example, a more efficient partition for very large circuits [35] is shown in Fig. 2. A sufficient condition for convergence in that case is that each of the nonlinear subcircuit blocks is locally passive.

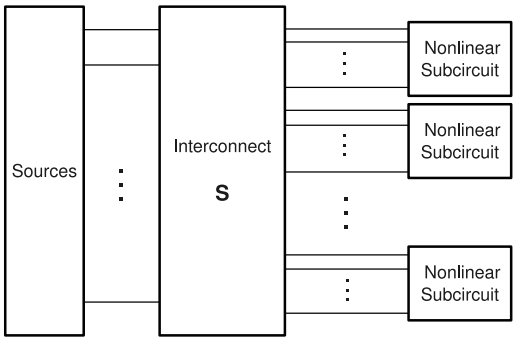

Figure 2: An alternate circuit partitioning

For nonconvergent circuits, it is possible to obtain convergence by reducing the time step size. All real nonlinear devices have internal parasitic capacitors in parallel with their ports. After time discretization, capacitors appear as conductances and have the effect of "passivizing" the nonlinear devices. The conductance is inversely proportional to the time step. It is always possible to reduce the time step until all devices become locally passive (a similar reasoning can be made with parasitic inductors in series). This result presented here is somewhat similar to the "capacitor to ground" condition for Iterated Timing Analysis and Waveform Relaxation methods [13]. However this approach is often not practical as the required time step becomes too small.

3.3 Convergence Acceleration

It is shown in Ref. [13] that when convergent, relaxation methods usually converge linearly as opposed to quadratic convergence rate with Newton's method. In the current implementation, a vector extrapolation method called Minimum Polynomial Extrapolation (MPE) [28] is applied to the vector sequence generated by Eq. (17) to accelerate the convergence rate. Assume here that the vector sequence is convergent to a fixed point. MPE is based on the differences of the vectors in the sequence. Define the following difference vector,

$$\mathbf{u}_n^k = \Delta \mathbf{b}_n^k = \mathbf{b}_n^{k+1} - \mathbf{b}_n^k$$

For a fixed integer K (usually $K << n_s$)we can define a $n_s \times K$ matrix whose columns are the vectors of differences:

$$\mathbf{U} \equiv \mathbf{U}_K = \left[\mathbf{u}_n^0,\ \mathbf{u}_n^1,\ \ldots,\ \mathbf{u}_n^{K-1}\right] \ . \tag{22}$$

Now a vector $\mathbf{q}_n = [q_n^0,\ q_n^1,\ \ldots,\ q_n^{K-1}]^T$ is defined as follows:

$$\mathbf{q}_n = -\mathbf{U}^+ \mathbf{u}_n^K \ , \tag{23}$$

where $\mathbf{U}^+$ is the pseudoinverse (or Moore-Penrose generalized inverse [42]) of $\mathbf{U}$. The computation of $\mathbf{q}_n$ requires the decomposition of $K \times K$ matrix. The extrapolated vector $\mathbf{b}_n^P$ is given by *Theorem 1* in [28].

$$\mathbf{b}_n^P = \frac{\sum_{k=0}^{K} q_n^k \mathbf{b}_n^k}{\left(\sum_{k=0}^{K} q_n^k\right)} \,. \tag{24}$$

The number of vectors to use in the extrapolation (K) should be set equal to the number of dominant eigenvalues of $[\mathbf{J}_f\mathbf{S}]$. If K is chosen properly MPE obtains the fixed point in one iteration for linear systems and converges quadratically for nonlinear systems, provided that the initial vector sequence is close to the solution. If K is too small, the extrapolated vector still get closer to the solution but convergence is slower [28]. Thus the combination of relaxation plus extrapolation may have a convergence performance comparable to Newton's method. In the present implementation K is set as simulation parameter.

The computational cost of an extrapolation is roughly equivalent to the cost of decomposing a square matrix of size $K \times K$. For medium and large circuits K is smaller than the number of nonlinear ports and this results in computational savings. It is interesting (but of little practical use) to note that MPE converges to the solution even if the original sequence is divergent [28], if the initial vector sequence is close enough to the solution.

4 Simulation Results

The transient analysis based on waves has been implemented in the *f*REEDA™ [27] simulator (type: *WaveTran*). A simplified pseudo-code for the WaveTran analysis is presented in Algorithm 1. Here, K is the number of vectors to extrapolate, *tol* is the predefined tolerance, h is the time step size and t_{end} is the simulation end time. All those are set as simulation parameters in WaveTran.

The performance of the proposed analysis is compared with the previously available state-variable transient analyses, types: *Tran* (uses a sparse-matrix formulation, see [38]) and *Tran2* (uses the formulation of Eq. (8), see [29]). Results from Tran and Tran2 are assumed to be correct, as these analysis has been previously verified against measurements and other circuit simulators [38, 40]. When possible, the times obtained with *ngspice* are also reported. Ngspice timings are expected to differ with any of the other timings as ngspice uses an adaptive time step algorithm, a different nonlinear model formulation and a different program architecture, but the results are still included in the table to be used as a well-known reference. The performance of the proposed method for different circuits is summarized in Table 1, all simulations are performed in Intel Core™ i7 CPU 2.8 GHz computer using fixed time step and the same absolute tolerance equal to 10^{-8}.

Algorithm 1 Transient Analysis based Fixed-Point iterations of Waves

calculate $\mathbf{M}_{sv}$
calculate $\mathbf{S}$ using Eq. (12)
repeat
  initial guess is set to the results in previous step
  update $\mathbf{s}_{sv,n}$
  calculate $\mathbf{a}_{0,n}$ using Eq. (13)
  repeat
    apply Eq. (17) for K iterations
    calculate $\mathbf{b}_n^P$ using Eq. (24)
    replace $\mathbf{b}$ by $\mathbf{b}_n^P$
  until $(error \leq tol)$
  increase time, $t = t + h$
until $(t < t_{end})$

Table 1: Summary of simulation results

Circuit	1. MESFET [37]	2. MMIC (Fig. 3)	3. Colpitts [39]	4. Soliton (Fig. 4)	5. Multi-MMIC (Fig. 5)	6. Power-Combiner (Fig. 6)
Nonlinear ports (n_s)	3	4	3	47	255	700
MNAM Size	17	555	7	2017	12860	21682
Reference Port resistance (Ω)	200	50	50	440	50	50
Input Power Level (dBm)	7	-13	-	30	19	6.5
Time Steps	200	1000	7500	5000	4000	1000
Iterations (WT-plain)	29	15	45	6	33	34
Iterations (WT)	12	7	10	5	13	12
K	4	4	4	2	4	6
Avg. extrap.	1.74	0.99	1.34	0.99	1.98	0.99
Newton Iter.	1.16	0.99	0.99	1.09	1.00	0.99
Simulation time (WT-Plain) s	0.2	1.65	23.8	55.76	1676.83	1932.47
Simulation time (WT) s	0.12	1.17	8.16	51.67	**734.93**	**805.33**
Simulation time (Tran) s	0.03	3	1	106	4060	1907
Simulation time (Tran2) s	0.02	0.41	0.74	30.39	1576	997.01
Simulation time (ngspice) s			0.14	31.69		

Circuit 1 is a single MESFET amplifier without thermal connection (Fig. 13 in [37]) and Circuit 2 (Fig. 3) is a model of the Filtronics LMA 411 X-band MMIC low noise amplifier (LNA) [38]. Circuit 3 is a Colpitts oscillator [39]. Circuit 4 (Fig. 4) is a nonlinear transmission line, or *soliton* line [40], composed of 47 diodes and 48 lossy transmission lines. Circuit 5 is shown in Fig. 5 and is composed of 5 MMIC LNA each connected to a soliton line (Circuit 4) at the output stage, each LNA fed with a different input frequency. Circuit 6 is an X-band MMIC array spacial power combiner [43]. Each HEMT finger is modelled independently in this circuit, therefore each amplifier contributes 28 state variables which results in 700 state variables for the complete circuit. The electromagnetic structures in this circuit are modelled in time-domain using a convolution approach as explained in Section 2. The Materka-Kacprzac Model is used for the MESFET in Circuit 1, the Curtice Ettemberg Model is used for the MESFETs in Circuit 2 and the Gummel-Poon model is for the BJT in Circuit 3. Netlists for some of these circuits are available in [30]. Values in the table are average per time step except *Newton Iteration*, this is the average value per relaxation iteration and the term *plain* refer to WaveTran (WT) without MPE. The reference resistance used for each simulation is shown in the table. In the current implementation this value is the same for all ports. This value has an effect in the convergence rate of the method, and the optimum convergence value changes with the operating point of the circuit. A method to determine the optimum value for each port has not been developed yet. The *Input Power Level* row shows the AC power level of the input sources referred to 50 Ω in all circuits except Circuit 6, which is referred to 20 Ω. The Iterations rows, (WT and WT-plain) compare the number of iterations needed for WaveTran with and without MPE. The last four rows compare the total running time using WaveTran (plain and with extrapolations) with Tran, Tran2, the standard state-variable transient analyses in *f*REEDA™ and, where possible, results from ngspice are also shown. It can be seen that in some cases extrapolations can decrease simulation times significantly, specially when many iterations per time step are required. For different circuits, all the simulated output voltages are compared with that from Tran2 and some zoom in plots are presented in Figs. 7, 8, 9 and 10. As expected the results from both simulation methods agree. Fig. 11 shows the convergence acceleration effect of MPE for Circuits 1 and 3. The plots show the error for iterations at one representative time step. For all simulations on average only one Newton iteration is necessary at the nonlinear device level. The average number of Newton iterations is slightly less than 1 for some circuits. That is because sometimes during the fixed-point iterations the stop criteria for the Newton method is satisfied by the initial guess and thus the Newton update is not performed. Thus the computational cost of using Newton's method to obtain reflected waves from nonlinear device models formulated in terms of voltages and currents is not too expensive.

It can be observed that for the circuits considered here Tran2 is faster than Tran even when Tran should scale better for large circuits due to the sparse formulation. The main reason for this is the efficiency gain of the matrix reduction approach (Eq. (8)) for circuits with many linear parasitics and relatively

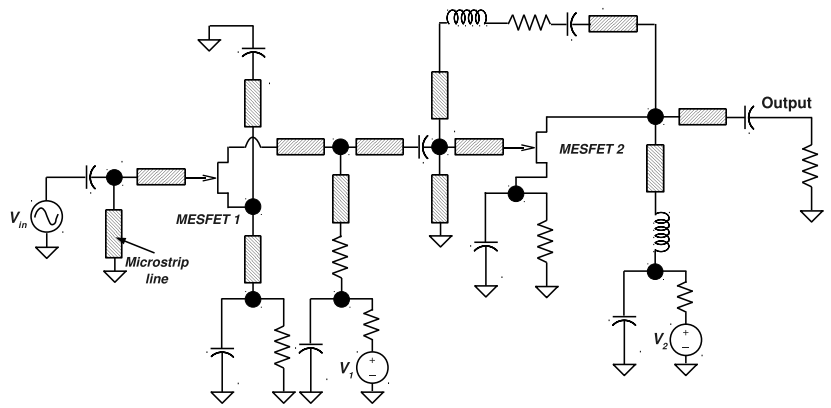

Figure 3: X-band MMIC LNA (LMA 411)

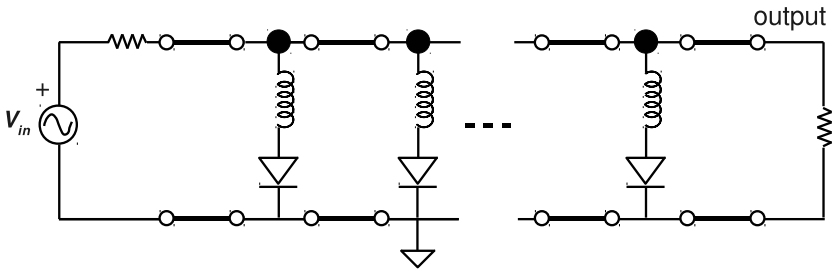

Figure 4: Nonlinear transimission line (soliton line)

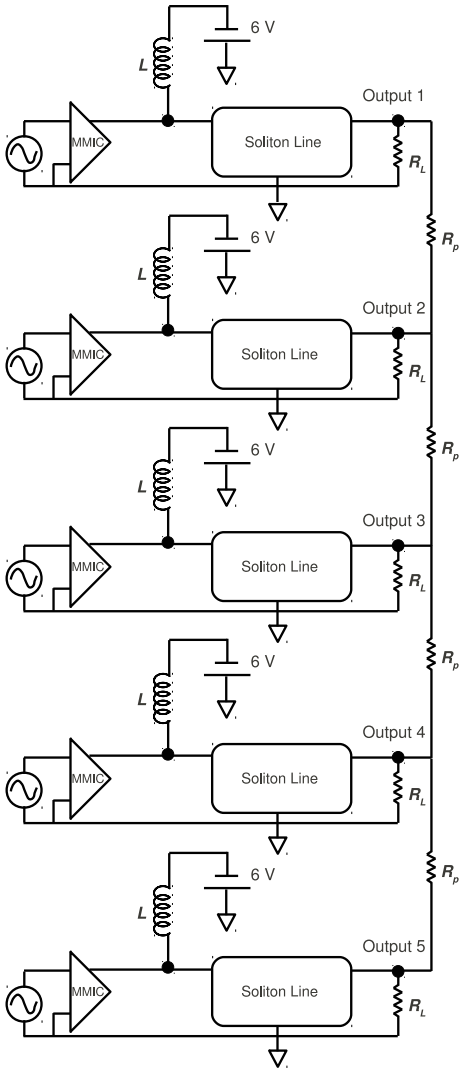

Figure 5: Multi MMIC-Soliton-line schematic

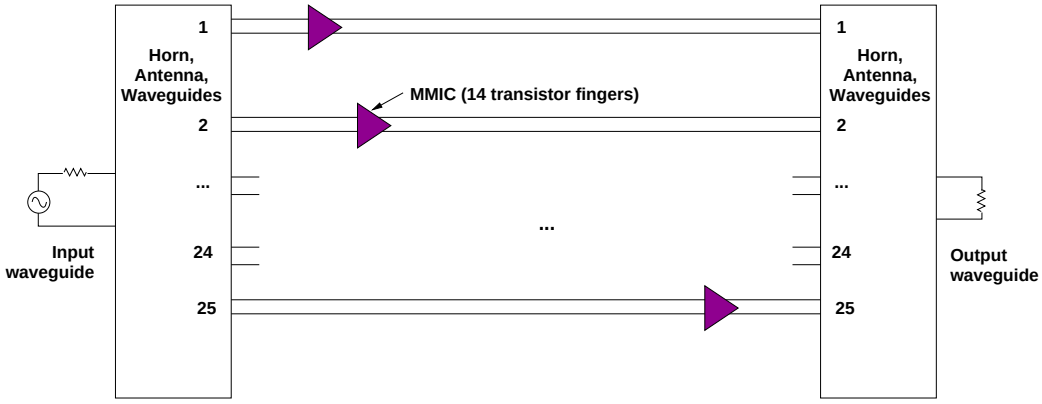

Figure 6: X-Band MMIC array spacial power combiner

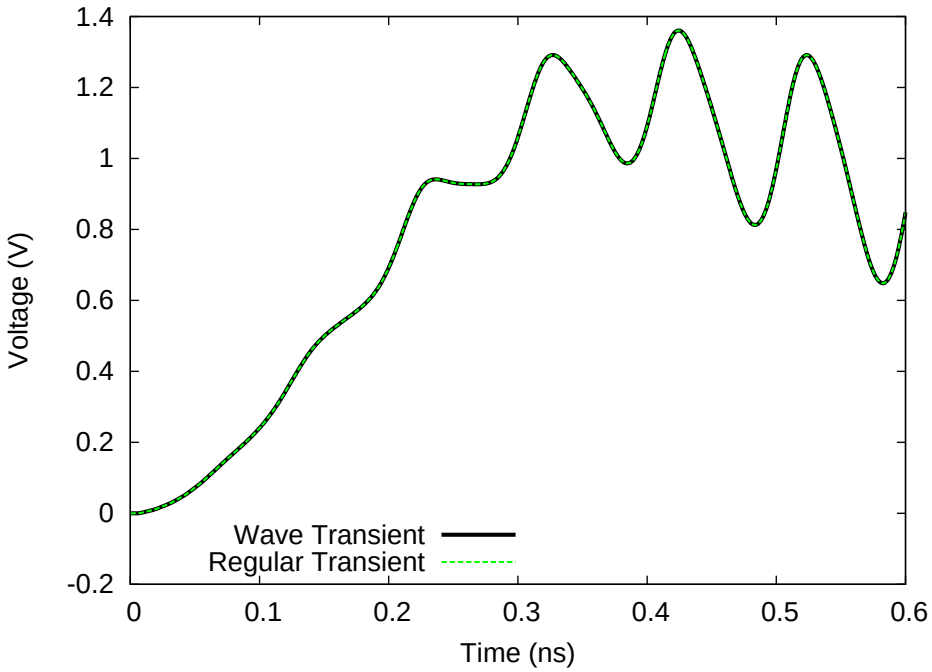

Figure 7: Output voltage of MMIC LNA

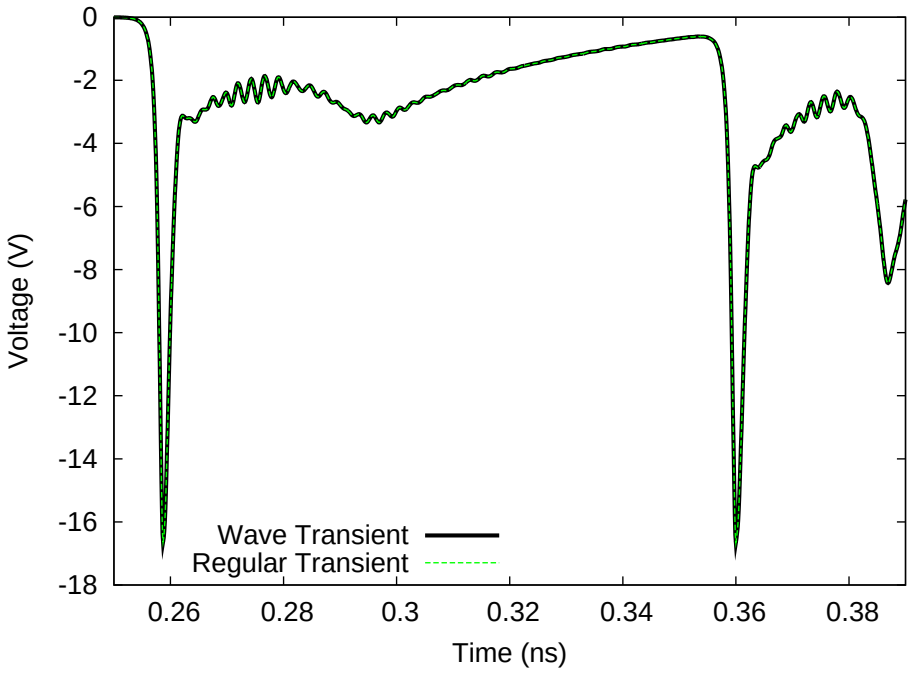

Figure 8: Output voltage of Soliton Line

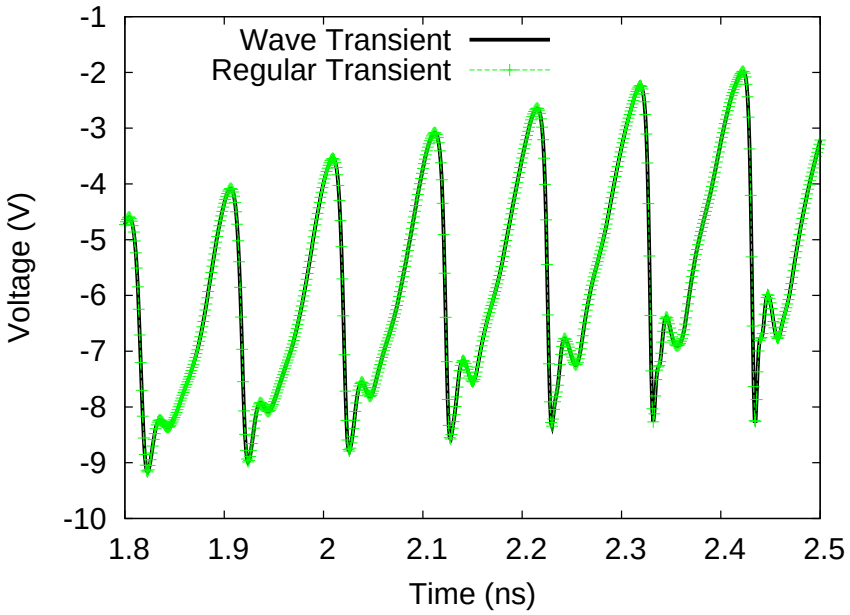

Figure 9: Voltage at Output 5 of the Multi MMIC-Soliton-line

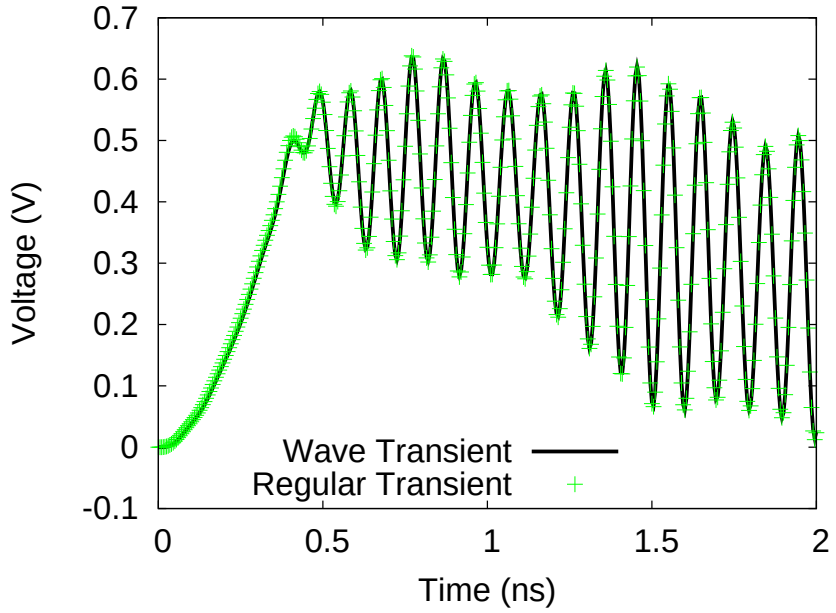

Figure 10: Output voltage of the X-Band MMIC array spacial power combiner

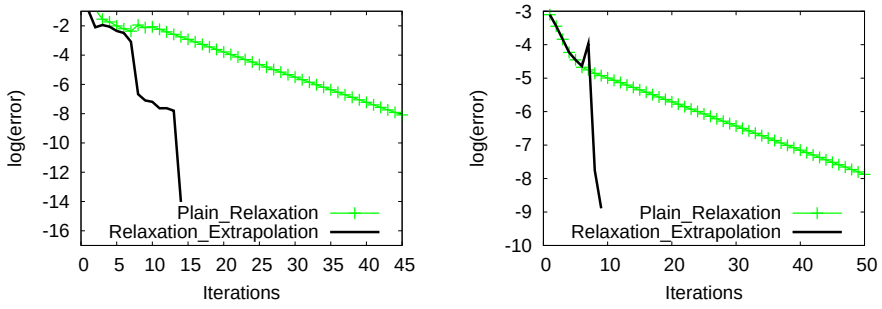

Figure 11: Comparison of errors for a single MESFET circuit and Colpitts Oscillator

few nonlinear ports, as it can be seen by comparing the Modified Nodal Admittance Matrix (MNAM) Size row and the Nonlinear Ports row. Taking this into account to evaluate the performance of relaxation based on waves, WaveTran should be compared with Tran2 as they share the same matrix reduction approach. WaveTran is slower than Tran2 for the smaller sample circuits but as the circuit size increases the method becomes more efficient. For Circuits 5 and 6 with 255 and 700 state variables, respectively, the proposed relaxation method is more efficient than Tran2 formulation as it does not require large matrix decompositions after $\mathbf{S}$ has been calculated.

5 Discussion and Future Research

A nonlinear transient analysis based on state variables and relaxation of waves has been presented for the first time. The application of MPE extrapolation to accelerate the convergence of this formulation was also reported here for the first time. The method is always convergent for circuits with passive linear and locally passive nonlinear devices. For circuits that contain mostly locally passive nonlinear devices or transistors separated by important passive networks the proposed method is often convergent. As the size of the circuit increases the performance becomes better than with a regular state-variable-based transient formulation.

Some issues that should be further investigated are a method to select optimum reference resistance values for each port and a way to ensure convergence in circuits with locally active nonlinear devices. As discussed in [2], the time step can be made variable in the proposed approach at the expense of one matrix decomposition (calculation of scattering matrix, $\mathbf{S}$) each time the step size is changed. For circuits that satisfy the convergence criteria, further research will investigate any performance gains achieved by reformulating the method using the alternate circuit partition (Fig. 2) and implementing a wave-based waveform relaxation approach.

Acknowledgments

The authors would like to thank the National Research Council of Canada (NSERC) for supporting this work and also would like to thank Dr. Michael B. Steer and the anonymous reviewers for their suggestions.

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