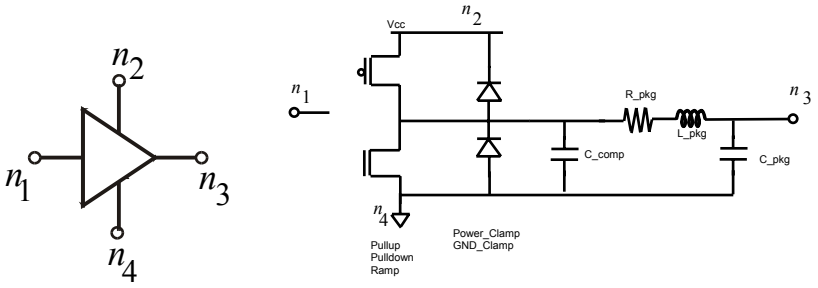

Description:
This element implements a behavioral model of a buffer based on the IBIS2 specification.

Form: ibis:<instance name> n_1 n_2 n_3 n_4 <parameter list>

n_1 is the input terminal,

n_2 unity voltage ramp source terminal,

n_3 is the output terminal,

n_4 is the reference terminal.

Parameters:

Parameter	Type	Default value	Required?
"ibis_file": IBIS filename given by user	TR_STRING	N/A	Yes
VCC : Given VCC (volts)	TR_DOUBLE	N/A	No

Example:
ibis:ibis1 4 3 2 0 ibis_file = "lsi.ibs" Vcc=3.3

Model Documentation:
$v_1=f_1(t)$ [from IBIS V-t (falling/Rising) table]
$Ipu=f_2(v_1)$ [from IBIS V-I Pullup table]
$Ipd=f_3(v_1)$ [from IBIS V-I Pulldown table]
$Igc=f_4(v_1)$ [from IBIS V-I Power Clamp table]
$Ipc=f_5(v_1)$ [from IBIS V-I Ground Clamp table]
$Kd=v_1/V_{cc}$
Ku= 1-Kd
Iout1 = (Ku * Ipu) + (Kd*Ipd) +Ipc +Igc

Sample Netlist:

```
vpulse:vramp1 3 0 v1=0v v2=1000000v td=0n tr=1000000n tf=0n pw=1000000000000ns per=1000000000000ns
*the upper line is REQUIRED AS Given for all instantiations of ibis buffer*


*input gate voltage
vpulse:vgsar 4 0 v1=0v v2=3.3v td=0n tr=1.2n tf=1.2n pw=0.5ns per=5ns

res:r3 2 0 r=10

ibis:ibiszz 4 3 2 0 ibis_file = "xyz.abc"
.tran2 tstop=3e-9 tstep=0.1e-9 out_steps=100
.end
```

References:

[1]. ANSI/EIA's IBIS home page, http://www.eigroup.org/ibis/ibis.htm

[2]. IBIS modeling Cookbook, http://www.eigroup.org/ibis/ckbook1.htm

[3]. IBIS Modeling Resources, http://www.mentor.com/icx/modeling/ibis_modeling.html

[4]. "The Development of Analog SPICE Behavioral Model Based on IBIS model", Yin Wang, Han Ngee Tan, Nanyang Technological university, Singapore. http://www.ntu.edu.sg/home/ehntan/glsvlsi.zip

[5]. "Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS", Peivand Tehrani,Yuzhe Chen and Jiayuan Fang, State University of New York at Binghamton, http://www.sigrity.com/papers/ectc96/ectc96ibis.pdf

[6]. "A Novel Extraction Method of Analog SPICE Behavioral Model from IBIS Model", Hwan-Mok Jung, Chang-Gene Woo, Pyung Choi , Jong-Hwa Kwon, Jae-Hoon Yun, Kyungpook National University.S.Korea. http://asiclab.knu.ac.kr/members_page/paper/Camera-ready%20Paper.pdf

Known Bugs:

1. The model is not valid for frequency analysis.
2. Does not include package parasitics: R_pkg, C_pkg, L_pkg, C_comp

Version: 2003.05.15

Credits:

Name	Affiliation
Ambrish Kant Varma ambrish@ieee.org	NC State University
Rubina Firdaus Ahmed rubina@ieee.org	NC State University
Nikhil R Mahajan nrm94ee330@hotmail.com	NC State University