MESFET Materka-Kacprzac Model **mesfetm**

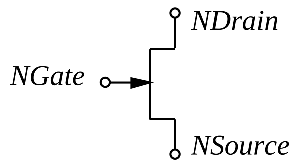

Figure 1: B — MESFET element.

fREEDA™ *Form:* `mesfetm:`⟨`instance name`⟩ n_1 n_2 n_3 ⟨`parameter list`⟩

n_1 is the drain node

n_2 is the gate node

n_3 is the source node

parameter list see table 1 for parameter list

n_1 is the drain node

n_2 is the gate node

n_3 is the source node

ModelName is the model name

Area is the optional relative area factor. (Units: none; Default: 1; Symbol:Area)

Example:

In fREEDA™*:*

```
mesfetm:b1 2 0 3
```

In `SPICE:`

```
B1  3  7  4 GAAS12 0.5
```

II The Materka-Kacprzac Model

Model Parameters:

Name	Description	Units	Default
AFAB	Slope factor of breakdown current ($AFAB$)	$1/V$	0.0
AFAG	Slope factor of gate conduction current ($AFAG$)	$1/V$	38.696
AREA	Area Multiplier ($AREA$)	-	1.0
C10	Gate source Schottky barrier capacitance for (C_{10})	F	0.0
CFO	Gate drain feedback capacitance for (C_{F0})	F	0.0
CLS	Constant parasitic component of gate-source capacitance (C_{LS})	F	0.0
E	Constant part of power law parameter (E)	-	2.0
GAMA	Voltage slope parameter of pinch-off voltage (γ)	$1/V$	0.0
IDSS	Drain saturation current for (I_{DSS})	A	0.1
IG0	Saturation current of gate-source Schottky barrier (I_{G0})	A	0.0
K1	Slope parameter of gate-source capacitance (K_1)	$1/V$	1.25
KE	Dependence of power law on V_{GS} , (K_E)	$1/V$	0.0
KF	Slope parameter of gate-drain feedback capacitance (K_F)	$1/V$	1.25
KG	Drain dependence on V_{GS} in the linear region, (K_G)	$1/V$	0.0
KR	Slope factor of intrinsic channel resistance (K_R)	$1/V$	0.0
RI	Intrinsic channel resistance for (R_I)	Ω	0.0
SL	Slope of the drain characteristic in the saturated region, (S_L)	S	0.15
SS	Slope of the drain characteristic in the saturated region (S_S)	S	0.0
T	Channel transit-time delay (τ)	s	0.0
VBC	Breakdown voltage (V_{BC})	V	10^{10}
VP0	Pinch-off voltage for (V_{P0})	V	-2.0

The physical constants used in the model evaluation are

k	Boltzman's constant	$1.3806226\,10^{-23}$ J/K
q	electronic charge	$1.6021918\,10^{-19}$ C

Standard Calculations

$$V_{TH} = (kT)/q \tag{1}$$

T is the analysis temperature

V_{DS}	Intrinsic drain source voltage
V_{GS}	Intrinsic gate source voltage
V_{GD}	Intrinsic gate drain voltage

Device Equations:

Current Characteristics

$$\begin{aligned} I_{DS} &= Area I_{DSS}\left[1 + S_S\frac{V_{DS}}{I_{DSS}}\right]\left[1 - \frac{V_{GS}(t-\tau)}{V_{P0}+\gamma V_{DS}}\right]^{(E + K_E V_{GS}(t-\tau))} \\ &\qquad \times\tanh\left[\frac{S_L V_{DS}}{I_{DSS}(1-K_G V_{GS}(t-\tau))}\right] \end{aligned} \tag{2}$$

$$I_{GS} = Area I_{G0}\left[e^{A_{FAG}V_{GS}} - 1\right] - I_{B0}\left[e^{-A_{FAB}(V_{GS}+V_{BC})}\right] \tag{3}$$

$$I_{GD} = Area I_{G0}\left[e^{A_{FAG}V_{GD}} - 1\right] - I_{B0}\left[e^{-A_{FAB}(V_{GD}+V_{BC})}\right] \tag{4}$$

$$R_I = \begin{cases} R_{10}(1-K_R V_{GS})/Area & K_R V_{GS} < 1.0 \\ 0 & K_R V_{GS} \ge 1.0 \end{cases} \tag{5}$$

Capacitance

$C_{LVL} = 1$ (default) for the standard Materka-Kacprzak capacitance model described below is used. The Materka-Kacprzak capacitances are

$$C'_{DS} = C_{DS} \tag{6}$$

$$C'_{GS} = \begin{cases} \left[C_{10}(1 - K_1 V_{GS})^{M_{GS}} + C_{1S}\right] & K_1 V_{GS} < F_{CC} \\ \left[C_{10}(1 - F_{CC})^{M_{GS}} + C_{1S}\right] & K_1 V_{GS} \geq F_{CC} \end{cases} \tag{7}$$

$$C'_{GD} = \begin{cases} Area\left[C_{F0}(1 - K_1 V_1)^{M_{GD}}\right] & K_1 V_1 < F_{CC} \\ Area\left[C_{F0}(1 - F_{CC})^{M_{GD}}\right] & K_1 V_1 \geq F_{CC} \end{cases} \tag{8}$$

Version:
2000.09.01

Credits:

Name	Affiliation	Date	Logo
Carlos E. Christofferson	NC State University	Sept 2000	NC STATE UNIVERSITY
www4.ncsu.edu/˜ cechrist			