

CMOS NOR Gate

cmosnor



Description:

This element models a CMOS NOR gate.

Form: `cmosnor:<instance name> n1 n2 n3 n4 n5 <parameter list>`

n1 is the high voltage source (Vdd) terminal,
n2 is the first input terminal,
n3 is the second input terminal,
n4 is the output terminal,
n5 is the ground or Vss terminal

Parameters:

Parameter	Type	Default Value	Required
vtn: NMOS Threshold Voltage (V)	TR_DOUBLE	1	No
vtp: PMOS Threshold Voltage (V)	TR_DOUBLE	-1	No
un: Effective Mobility of Electrons in NMOS ((cm ²)/(V-sec))	TR_DOUBLE	500	No
up: Effective Mobility of Electrons in PMOS ((cm ²)/(V-sec))	TR_DOUBLE	200	No
en: Permittivity of the Gate Insulator in NMOS (F/cm)	TR_DOUBLE	34.515e-14	No
ep: Permittivity of the Gate Insulator in PMOS (F/cm)	TR_DOUBLE	34.515e-14	No
tox: Thickness of the Gate Insulator (cm)	TR_DOUBLE	2.0e-6	No
wn: Channel Width of NMOS (cm)	TR_DOUBLE	50e-6	No
ln: Channel Length of NMOS (cm)	TR_DOUBLE	2.0e-6	No
wp: Channel Width of PMOS (cm)	TR_DOUBLE	50e-6	No
lp: Channel Length of PMOS (cm)	TR_DOUBLE	2.0e-6	No
td: Response Delay Time (sec)	TR_DOUBLE	0	No

Example:

`cmosnor:nor1 1 2 3 4 0 td=0.1e-6`

Notes:

This is an analog implementation of a digital NOR gate.

Known Bugs:
No known bugs.

Model documentation:

$\beta_n = (\text{un})(\text{en})(\text{wn})/(\text{tox})(\text{ln})$
 $\beta_p = (\text{up})(\text{ep})(\text{wp})/(\text{tox})(\text{lp})$

The operation of the CMOS NOR gate can be divided into five regions:
 V_{in} is considered to be the dominant input of V_{in1} and V_{in2}

Region A: $0 < V_{in} < V_{Tn}$
PMOS: nonsaturated; NMOS cutoff
 $V_{out} = V_{DD}$
 $I_{DSn} = I_{DSp} = 0$

Region B: $V_{Tn} < V_{in} < V_{DD}/2$
PMOS: nonsaturated; NMOS saturated
 $I_{DSp} = -\beta_p [(V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{out}) - (0.5)(V_{DD} - V_{out})^2]$
 $I_{DSn} = -I_{DSp}$
 $V_{out} = (V_{in} - V_{Tp}) + \text{sqrt}[(V_{in} - V_{Tp})^2 - 2 V_{DD} (V_{in} - 0.5V_{DD} - V_{Tp}) - (\beta_n / \beta_p) [(V_{in} - V_{Tp})^2]$

Region C: $V_{in} = V_{DD}/2$
PMOS: saturated; NMOS saturated
 $I_{DSp} = -0.5\beta_p [(V_{in} - V_{DD} - |V_{Tp}|)^2]$
 $I_{DSn} = -I_{DSp}$
 $V_{in} - V_{Tn} < V_{out} < V_{in} - V_{Tp}$

Region D: $V_{DD}/2 < V_{in} < V_{DD} + V_{Tp}$
PMOS: saturated; NMOS nonsaturated
 $I_{DSp} = -0.5\beta_p [(V_{in} - V_{DD} - |V_{Tp}|)^2]$
 $I_{DSn} = -I_{DSp}$
 $V_{out} = (V_{in} - V_{Tn}) + \text{sqrt}[(V_{in} - V_{Tn})^2 - (\beta_p / \beta_n) [(V_{in} - V_{DD} - V_{Tp})^2]$

Region E: $V_{in} > V_{DD} + V_{Tp}$
PMOS: cutoff; NMOS nonsaturated
 $V_{out} = V_{SS}$

References:

Weste and Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, 1994
G.M. Glasford, *Digital Electronic Circuits*, Prentice-Hall, 1988

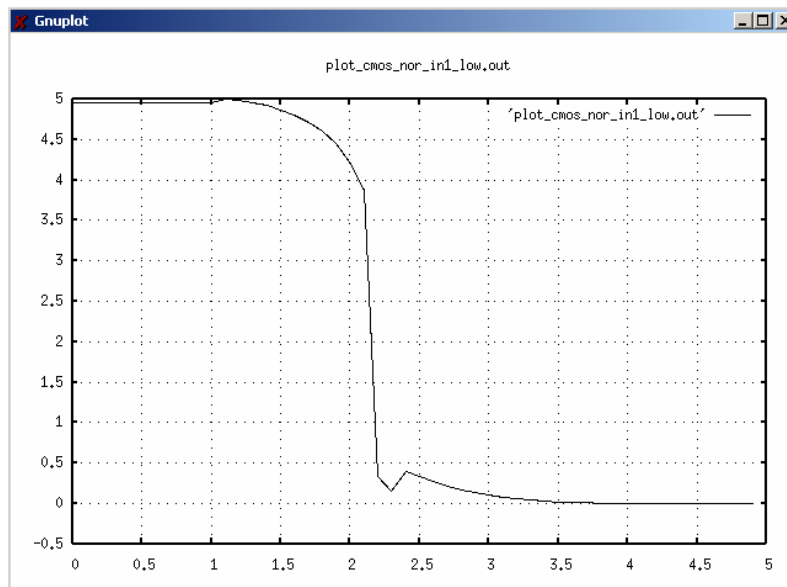
Sample Netlist:

The following netlist plots the output voltage of the CMOS gate for an input voltage range of 0 ~ 5V for V_{in2} and constant $V_{in1} = 0V$.

```
* CMOS NOR Gate Test
.dc sweep="vsource:Vin2" start=0 stop=5 step=0.1
vsource:Vdd 1 0 vdc=5
vsource:Vin1 2 0 vdc=0
vsource:Vin2 3 0
cmosnor:nor 1 2 3 4 0
res:R 4 0 r=1000000
.out plot term 4 vt in "plot_cmos_nor_in1_low.out"
.end
```

Validation:

The output graph from the above netlist is shown below:



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Credits:

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