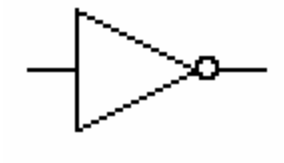
CMOS Inverter cmosinv



Description:
This element models a CMOS inverter gate.

Form: cmosinv:<instance name> *n1 n2 n3 n4* <parameter list>

n1 is the high voltage source (Vdd) terminal,
n2 is the input terminal,
n3 is the output terminal,
n4 is the ground or Vss terminal.

Parameters:

Parameter	Type	Default Value	Required
vtn: NMOS Threshold Voltage (V)	TR_DOUBLE	1	No
vtp: PMOS Threshold Voltage (V)	TR_DOUBLE	-1	No
un: Effective Mobility of Electrons in NMOS ((cm^2)/(V-sec))	TR_DOUBLE	500	No
up: Effective Mobility of Electrons in PMOS ((cm^2)/(V-sec))	TR_DOUBLE	200	No
en: Permittivity of the Gate Insultor in NMOS (F/cm)	TR_DOUBLE	34.515e-14	No
ep: Permittivity of the Gate Insultor in PMOS (F/cm)	TR_DOUBLE	34.515e-14	No
tox: Thickness of the Gate Insulator (cm)	TR_DOUBLE	2.0e-6	No
wn: Channel Width of NMOS (cm)	TR_DOUBLE	50e-6	No
ln: Channel Length of NMOS (cm)	TR_DOUBLE	2.0e-6	No
wp: Channel Width of PMOS (cm)	TR_DOUBLE	50e-6	No
lp: Channel Length of PMOS (cm)	TR_DOUBLE	2.0e-6	No
td: Response Delay Time (sec)	TR_DOUBLE	0	No

Example:
cmosinv:inverter1 1 2 3 0 td=0.1e-6

Notes:
This is an analog implementation of a digital inverter gate.

Known Bugs:
No known bugs.

Model documentation:

ßn = (un)(en)(wn)/(tox)(ln)
ßp = (up)(ep)(wp)/(tox)(lp)

The operation of the CMOS inverter can be divided into five regions:

Region A: $0 < Vin < V_{Tn}$
PMOS: nonsaturated; NMOS cutoff
$V_{out} = V_{DD}$
$I_{DSn} = I_{DSp} = 0$

Region B: $V_{Tn} < Vin < V_{DD}/2$
PMOS: nonsaturated; NMOS saturated
$I_{DSp} = - ßp [(V_{DD} - Vin - |V_{Tp}|)(V_{DD} - Vout) – (0.5)(VDD - Vout)^2]$
$I_{DSn} = - I_{DSp}$
$V_{out} = (V_{in} – V_{Tp}) + sqrt[(V_{in} – V_{Tp})^2 – 2 V_{DD} (V_{in} – 0.5V_{DD} - V_{Tp}) – (ßn/ ßp) [(V_{in} – V_{Tp})^2]$

Region C: $Vin = V_{DD}/2$
PMOS: saturated; NMOS saturated
$I_{DSp} = - 0.5ßp [(Vin - V_{DD} - |V_{Tp}|)^2]$
$I_{DSn} = - I_{DSp}$
$V_{in} – V_{Tn} < V_{out} < V_{in} – V_{Tp}$

Region D: $V_{DD}/2 < Vin < V_{DD} + V_{Tp}$
PMOS: saturated; NMOS nonsaturated
$I_{DSp} = - 0.5ßp [(Vin - V_{DD} - |V_{Tp}|)^2]$
$I_{DSn} = - I_{DSp}$
$V_{out} = (V_{in} – V_{Tn}) + sqrt[(V_{in} – V_{Tn})^2 – (ßp/ ßn) [(V_{in} – V_{DD} - V_{Tp})^2]$

Region E: $Vin > V_{DD} + V_{Tp}$
PMOS: cutoff; NMOS nonsaturated
$V_{out} = Vss$

References:

Weste and Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, 1994
G.M. Glasford, *Digital Electronic Circuits*, Prentice-Hall, 1988

Sample Netlist:

The following netlist plots the output voltage of the CMOS gate for an input voltage range of 0 ~ 5V.

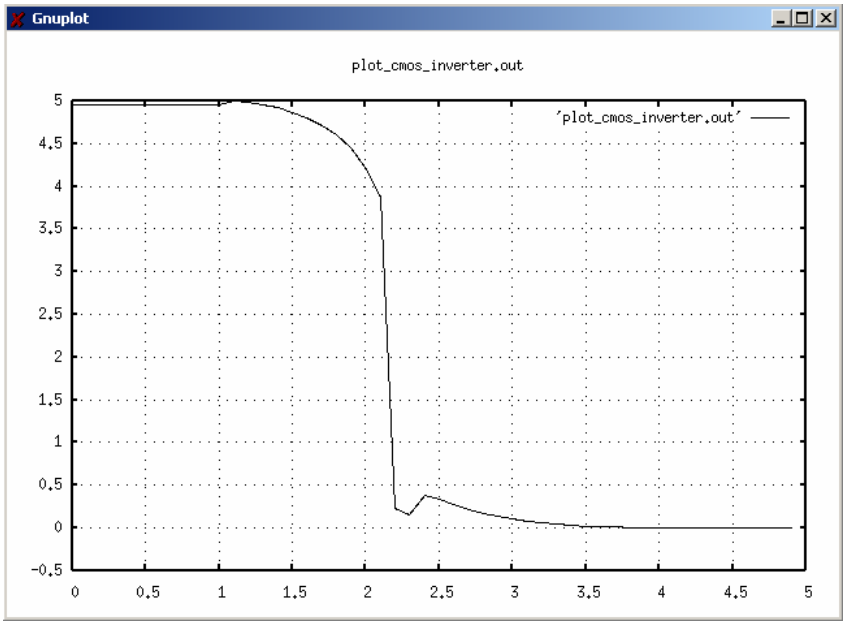
```
* CMOS Inverter Test

.dc sweep="vsource:Vin" start=0 stop=5 step=0.1

vsource:Vdd 1 0 vdc=5
vsource:Vin 2 0
cmosinv:inverter 1 2 3 0 tr=0.5 tf=0.5
res:R 3 0 r=1000000

.out plot term 3 vt in "plot_cmos_inverter.out"
.end
```

Validation:
The output graph from the above netlist is shown below:



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Credits:

Name	Affiliation	Date	Links
Mazen M Kharbutli	NCSU	April, 2003	http://www4.ncsu.edu/~mmkharbu
mazen_kharbutli@yahoo.com			