CMOS NOR Gate with Junction temperature cmosnort

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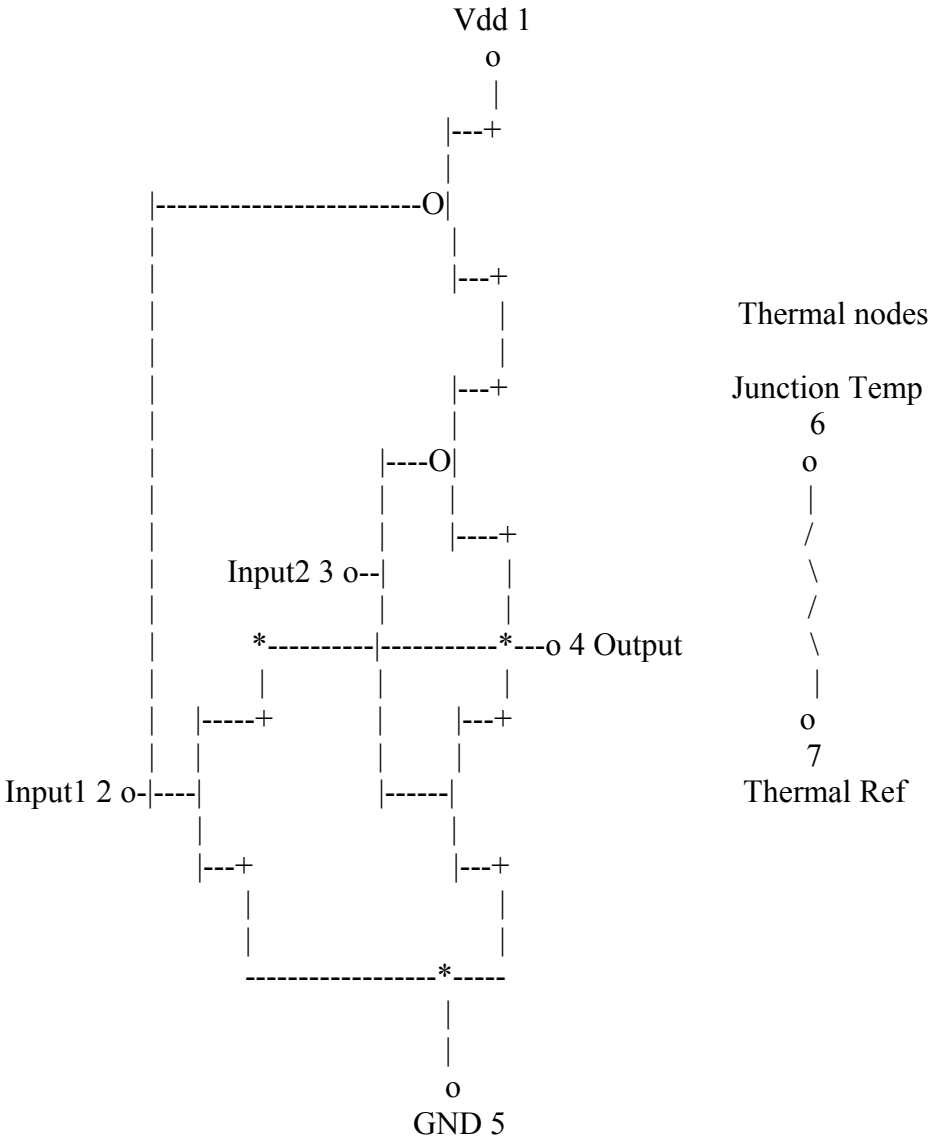

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Description:
This element implements a generic CMOS NOR gate and calculates junction temperature.

Form: cmosnort: <instance name> n_1 n_2 n_3 n_4 n_5 n_6 n_7 <parameter list>

instance name is the model name

n_1 is the NOR element Vdd node,

n_2 is the NOR element input 1 node,

n_3 is the NOR element input 2 node,

n_4 is the NOR element output node,

n_5 is the NOR element Ground node,

n_6 is the NOR element Junction temperature node,

n_7 is the NOR element Thermal Reference node.

Parameters:

Parameter	Type	Default value	Required?
vtn: NMOS threshold voltage (V)	DOUBLE	1	no
vtp: PMOS threshold voltage (V)	DOUBLE	-1	no
un: effective mobility of electrons in NMOS (cm^2)/(V-sec)	DOUBLE	500	no
up: effective mobility of holes in PMOS (cm^2)/(V-sec)	DOUBLE	200	no
en: permittivity of gate insulator in NMOS (F/cm)	DOUBLE	34.515e-14	no
ep: permittivity of gate insulator in PMOS (F/cm)	DOUBLE	34.515e-14	no
tox: thickness of gate insulator (cm)	DOUBLE	2e-6	no
wn: channel width of NMOS (cm)	DOUBLE	50e-6	no
ln: channel length of NMOS (cm)	DOUBLE	2e-6	no
wp: channel width of PMOS (cm)	DOUBLE	100e-6	no
lp: channel length of PMOS (cm)	DOUBLE	2e-6	no

td: response delay time (sec)	DOUBLE	0	no
thermal: thermal element flag	BOOLEAN	False	no
tnom: nominal temperature (K)	DOUBLE	300	no
zt: thermal impedance summation (K/W)	DOUBLE	310	no
c1: PMOS GS capacitance (F)	DOUBLE	1e-12	no
c2: NMOS GS capacitance (F)	DOUBLE	1e-12	no
c3: output GS (Miller) capacitance (F)	DOUBLE	1e-12	no
c4: parasitic diode capacitance from output to Vdd (F)	DOUBLE	1e-12	no
c5: parasitic diode capacitance from output to Ground (F)	DOUBLE	1e-12	no
freq: operating frequency (Hz)	DOUBLE	1e6	no
lk: leakage current (A)	DOUBLE	8e-6	no

Example:
cmosnort:nor 1 2 3 4 0 1000 "tref"

Model Documentation: (Start on a new page, Include English and make sure font sizes are consistent. Use figures if necessary. Please avoid using scanned image.)

MOSFET cutoff current I_{ds}, for $V_{gs} < V_t$:

$$I_{ds} = 0$$

MOSFET current factor β:

$$\beta = \mu * C_{ox} * (W / L)$$

MOSFET linear current I_{ds}, for $V_{gs} - V_t > V_{ds} > 0$:

$$I_{ds} = \beta * (V_{gs} - V_t - (V_{ds} / 2)) * V_{ds}$$

MOSFET saturation current I_{ds}, for $V_{ds} > V_{gs} - V_t > 0$:

$$I_{ds} = (\beta / 2) * (V_{gs} - V_t)^2$$

Power dissipation P_D:

$$P_D = (V_{sd,pmos} * I_{sd,pmos}) + (V_{ds,nmos} * I_{ds,nmos}) + (2 * freq * C * V_{dd}) + leakage$$

Junction temperature T_j:

$$T_j = T_{ambient} + (P_D * \theta_{jA})$$

References:

1. Mazen M Kharbutli. fREEDA element moscnor.
DEFAULT_ADDRESS"elements/Moscnor.h.html"

Sample Netlist:

```
* DC thermal CMOS NOR Test
* DC sweep input 1 voltage from 0 to 5V

.dc sweep="vsource:Vin" start=0 stop=5 step=0.1

.options iniTmp=300

.ref "tref"
.ref 0

vsource:Vdd 1 0 vdc=5
vsource:Vin 2 0
vsource:Vdd2 3 0 vdc=0

cmosnort:nor 1 2 3 4 0 1000 "tref" thermal=1
res:R 4 0 r=1000000

***thermal circuit
res:R1 1000 1001 r=6e3
```

```
vsource:t1 1001 "tref" vdc=iniTmp
cap:c1 1000 1001 c=1e-12

.out plot term 4 vt in "nor_voltage.out"
.out plot element "cmosnort:nor" 0 it in "nor_current.out"
.out plot element "cmosnort:nor" 4 ut in "nor_temperature.out"

.end
```

Validation:

This thermal CMOS NOR model adds thermal junction temperature calculation to the existing electrical CMOS NOR model (moscnor). Simulations were performed using the existing moscnor model in a netlist with a DC sweep from 0 to 5 Volts at the one input terminal. The second input terminal was connected to ground. The resulting output voltage and current was recorded. The thermal CMOS NOR model (cmosnort) was validated by making a new netlist with the cmosnort model. The resulting cmosnort voltage output and current output was compared to those of the original moscnor model and identical electrical results were obtained. The resulting cmosnort junction temperature data was empirically verified by correlating junction temperature data points with manually calculated results.

The original moscnor model uses a default parameter of wp = 50e-6 cm (channel width of PMOS). If this default parameter is used an erroneous element current output results. The cmosnort model uses a default parameter of wp = 100e-6 cm, resulting in an expected element current output.

Known Bugs:

None.

Credits:

Name	Affiliation	Date	Links
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