Motorola's Electro Thermal (MET) LDMOS Model MosnldMet

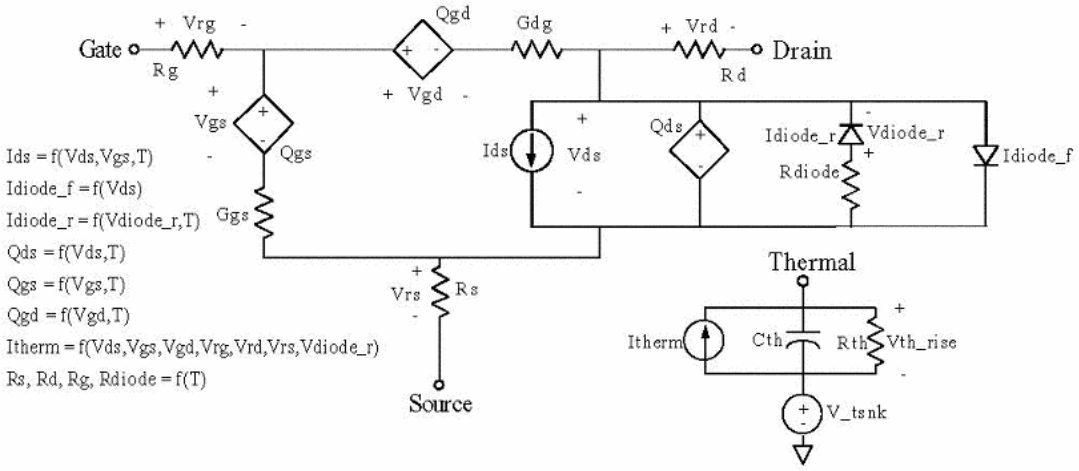


Figure 1. Large Signal Equivalent Circuit of the MET LDMOS model.

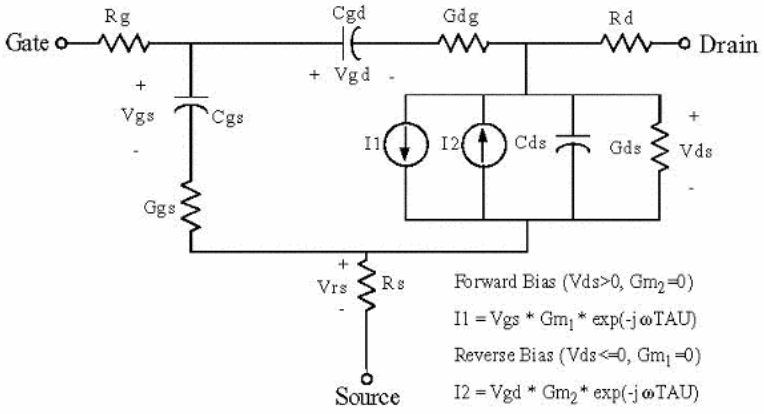


Figure 2. Isothermal Small Signal Equivalent Circuit of the MET LDMOS model.

Description:

This element implements Motorola's LDMOS. This is an electro thermal model that accounts for dynamic self-heating effects and was specifically tailored to model high power RF LDMOS transistors used in base station, digital broadcast, land mobile and subscriber applications.

Form: MosnldMet:`<instance name> n1 n2 n3 n4 n5 <parameter list>`

n1 is the gate terminal.
n2 is the drain terminal.
n3 is the source terminal.
n4 is the first thermal terminal.
n5 is the second thermal terminal.

Parameters:

Parameter	Type	Default value	Required?
RG_0	Double	1 ohm	Yes
RG_1	Double	.0001 ohm/K	Yes
RS_0	Double	.1 ohm	Yes
RS_1	Double	.0001 ohm/K	Yes
RD_0	Double	1.5 ohm	Yes
RD_1	Double	.0015 ohm/K	Yes
VTO_0	Double	3.5 V	Yes
VTO_I	Double	-.0001 V/K	Yes
Gamma	Double	-.02	Yes
VST	Double	.15 V	Yes
BETA_0	Double	.2 1/ohms	Yes
BETA_1	Double	-.0002 1/(ohms*K)	Yes
LAMBDA	Double	-.00025 1/V	Yes
VGEXP	Double	1.1	Yes
ALPHA	Double	1.5	Yes
VK	Double	7.0 V	Yes
DELTA	Double	.9 V	Yes
VBR_0	Double	75 V	Yes
VBR_1	Double	.01 V/K	Yes
K1	Double	1.5	Yes
K2	Double	1.15 1/V	Yes
M1	Double	9.5	Yes
M2	Double	1.2 1/V	Yes
M3	Double	.001	Yes
BR	Double	.5 1/(V*ohms)	Yes
RDIODE_0	Double	.5 ohm	Yes
RDIODE_1	Double	.001 ohm/K	Yes
ISR	Double	1e-13 A	Yes
NR	Double	1.0	Yes
VTO_R	Double	3.0 V	Yes
RTH	Double	10 degree C/watts	Yes
GGS	Double	1e5 1/ohms	Yes
GGD	Double	1e5 1/ohms	Yes
TAU	Double	1e-12 seconds	Yes
TNOM	Double	298 K	Yes
TSNK	Double	25 degrees C	Yes
CGST	Double	.001 1/K	Yes
CDST	Double	.001 1/K	Yes
CGDT	Double	0.0 1/K	No
CTH	Double	0.0 J/ degrees C	No
KF	Double	0.0	No

AF	Double	1.0	Yes
FFE	Double	1.0	Yes
N	Double	1.0	Yes
ISS	Double	1e-13 A	Yes
CGS1	Double	2e-12 F	Yes
CGS2	Double	1e-12 F	Yes
CGS3	Double	-4.0 V	Yes
CGS4	Double	1e-12	Yes
CGS5	Double	.25 1/V	Yes
CGS6	Double	3.5 1/V	Yes
CGD1	Double	4e-13 F	Yes
CGD2	Double	1e-13 F	Yes
CGD3	Double	.1 1/V^2	Yes
CGD4	Double	4 V	Yes
CDS1	Double	1e-12 F	Yes
CDS2	Double	1.5e-12 F	Yes
CDS3	Double	.1 1/V^2	Yes
N_FING	Double	1	Yes
Area	Double	1	Yes

Example:
MosnldMet:ldmos1 3 2 1 1000 “tref”

Model Documentation:

The MET LDMOS model is an electro thermal model that can account for dynamic self-heating effects and was specifically tailored to model high power RF LDMOS transistors used in base station, digital broadcast, land mobile and subscriber applications.

The MET LDMOS is a large signal nonlinear model. It includes static and dynamic thermal dependencies. The model is now capable of accurately representing the current-voltage characteristics and their derivatives at any bias point and operating temperature. Motorola developed a model capable of modeling a single continuously differentiable drain current, which models the sub threshold, triode, high current saturation and drain to source breakdown regions of operation. These parameters were developed by measuring the nonlinear drain current under pulsed voltage conditions at different operation temperatures, ensuring an isothermal measurement environment.

The model has three voltage and temperature dependent nonlinear charges, *Qgs*, *Qgd*, and *Qds*. *Ggs* and *Gdg* are two internal gate conductances with three dependent parasitic resistances, *Rg*, *Rd*, and *Rs*. The power rise is calculated with the use of the thermal sub-circuit. *Itherm* is the total instantaneous power dissipated in the transistor, *Rth* is the thermal resistance, *Cth* is the thermal capacitance, and *V_tsnk* is the voltage source that represents the heat sink temperature of the system.

Scaling Rules

The model parameters are scaled by two different parameters, *AREA*, which is the ratio of the desired gate periphery to the gate periphery of the transistor used in the extraction of the model parameters, and *N_FING*, which is the ratio of the desired number of fingers to the number of fingers of the transistor used in the extraction of the model parameters.

$$AREA = \frac{Znew}{Zextracted}$$

$$N\_FING = \frac{NGates\_extracted}{NGates\_new}$$

where *Znew* and *Ngates_new* are the gate periphery and number of gate fingers respectively of the desired transistor, and *Zextracted* and *Ngates_extracted* are the gate periphery and number of gate fingers of the extracted transistors.

$$RD\_0 = \frac{RD\_0}{AREA}$$

$$RS\_0 = \frac{RS\_0}{AREA}$$

$$RG\_0 = RG\_0 * AREA * N\_FING^2$$

$$RD\_1 = \frac{RD\_1}{AREA}$$

$$RS\_1 = \frac{RS\_1}{AREA}$$

$$RG\_1 = RG\_1 * AREA * N\_FING^2$$

$$RDSO\_0 = \frac{RDSO\_0}{AREA}$$

$$GGD = GGD * AREA$$

$$GGS = GGS * AREA$$

$$RTH\_0 = \frac{RTH\_0}{AREA}$$

$$C\_TH = C\_TH * AREA$$

$$BETA\_0 = BETA\_0 * AREA$$

$$BETA\_1 = BETA\_1 * AREA$$

$$CGS1 = CGS1 * AREA$$

$$CGS2 = CGS2 * AREA$$

$$CGS4 = CGS4 * AREA$$

$$CGD1 = CGD1 * AREA$$

$$CGD2 = CGD2 * AREA$$

$$CDS1 = CDS1 * AREA$$

$$CDS2 = CDS2 * AREA$$

$$ISS = ISS * AREA$$

$$ISR = ISR * AREA$$

$$BR = BR * AREA$$

$$RDIODE\_0 = \frac{RDIODE\_0}{AREA}$$

$$RDIODE\_1 = \frac{RDIODE\_1}{AREA}$$

MET LDMOS Model Equations

The temperature dependency of parasitic resistances is given by:

$$Rg = RG\_0 + RG\_1 * (T - TNOM)$$

$$Rd = RD\_0 + RD\_1 * (T - TNOM)$$

$$Rs = RS\_0 + RS\_1 * (T - TNOM)$$

$$T = Vth\_rise + TSNK + 273$$

where T is the actual or total temperature (not the temperature rise) in K and *TNOM* is the temperature at which the parameters were extracted. The value of *V_tsnk*(℃)is numerically equal to the heat sink temperature *TSNK*(℃). Notice that even though *RG_1*, *RD_1* and *RS_1* have units of Ω/K, their numerical value will be the same if the units are Ω/℃.

The forward bias drain to source current equation is given by:

$$Vto\_f = VTO\_0 + VTO\_1 * (T - TNOM)$$

$$Beta = BETA\_0 + BETA\_1 * (T - TNOM)$$

$$Vbr = VBR\_0 + VBR\_1 * (T - TNOM)$$

To maintain small signal to large signal model consistency, the gate to source voltage used in the calculation of the large signal drain to source current is delayed *TAU* seconds.

$$Vgs\_delayed(t) = Vgs(t - TAU)$$

$$Vgst2 = Vgs\_delayed - (Vto\_f + (GAMMA * Vds))$$

$$Vgst1 = Vgst2 - \frac{1}{2}(Vgst2 + \sqrt{(Vgst2 - VK)^2 + DELTA^2} - \sqrt{VK^2 + DELTA^2}$$

$$Vgst = VST * \ln(e^{\frac{Vgst1}{VST}} + 1)$$

$$Vbreff = \frac{Vbr}{2}(1 + Tanh[M1 - Vgst * M2])$$

$$Vbreff1 = \frac{1}{K2}(Vds - Vbreff) + M3(\frac{Vds}{Vbreff})$$

$$Ids = (Beta)(Vgst^{VGXEP})(1 + LAMBDA * Vds)Tanh\left[\frac{Vds * ALPHA}{Vgst}\right](1 + K1 * e^{Vbreff1})$$

The forward bias drain to source diode is given by:

$$Vt = \frac{k * T}{q}$$

where k is the boltzmann's constant(1.381e-23 J/K), T is the temperature in Kelvin, and q is the electron charge(1.602E-19C)

$$Idiode\_f = ISS(e^{\frac{Vds-Vbr}{N*Vt}})$$

The reverse bias drain to source vurrent equation is given by:

$$Vto\_r = VTO\_R + VTO\_1 * (T - TNOM)$$

$$Vgst2 = Vgs\_delayed - (Vto\_r - (GAMMA * Vds)$$

$$Vgst1 = Vgst2 - \frac{1}{2}(Vgst2 + \sqrt{(Vgst2 - VK)^2 + DELTA^2} - \sqrt{VK^2 + DELTA^2}$$

$$Vgst = VST * \ln(e^{\frac{Vgst1}{VST}} + 1)$$

$$Ids = (BR)(Vds)(Vgst)$$

The reverse bias drain to source diode is given by

$$Vt2 = \frac{k * T}{q}$$

$$Ism = ISR * (\frac{T}{TNOM})^{\frac{3}{NR}} e^{((\frac{-Eg}{NR*Vt2})*(1-\frac{T}{TNOM}))}$$

where Eg is the energy gap for silicon which is equal to 1.11 and T is the temperature in Kelvin.

$$Idiode\_r = Ism(e^{\frac{Vdiode\_r}{NR*Vt2}} - 1)$$

The reverse diode's series resistances is given by:

$$Rdiode = RDIODE\_0 + RDIODE\_1 * (T - TNOM)$$

The gate to source capacitance equation is given by:

$$Cgs = (CGS1 + CGS2 * [1 + Tanh(CGS6 * (Vgs + CGS3))] + CGS4 * [1 - Tanh(Vgs * CGS5)]) * (1 + CGST * (T - TNOM))$$

The gate to drain capacitance equation is given by

$$Cgd = (CGD1 + \frac{CGD2}{1 + CGD3 * (Vgd - CGD4)^2}) * (1 + CGDT * (T - TNOM))$$

The drain to source capacitance equation is given by

$$Cds = (CDS1 + \frac{CDS2}{1 + CDS3 * Vds^2}) * (1 + CDST * (T - TNOM))$$

To avoid convergence problems the maximum tempereture rise, *Vth_rise*(℃) is limited to 300 ℃ using the following equation:

$$Vth\_rise = \begin{cases} 0 & 0 \le Vth\_rise \\ Vth\_rise & 0 < Vth\_rise < 250 \\ 250 + 50 * \tanh(\frac{Vth\_rise - 250}{50}) & 250 \le Vth\_rise \end{cases}$$

References:

[1] W. Curtice, J. Pla, D. Bridges, T. Liang & E. Shumate, A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF LDMOS FETs, 1999 IEEE MTT-S International Microwave Symposium, Anaheim CA, pp. 419-422

[2] M. Golio, Microwave MESFETs and HEMTs, Arthec House, Boston, 1991, pp. 79-80

[3] P. Antognetti & G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw Hill, New York, 1998.

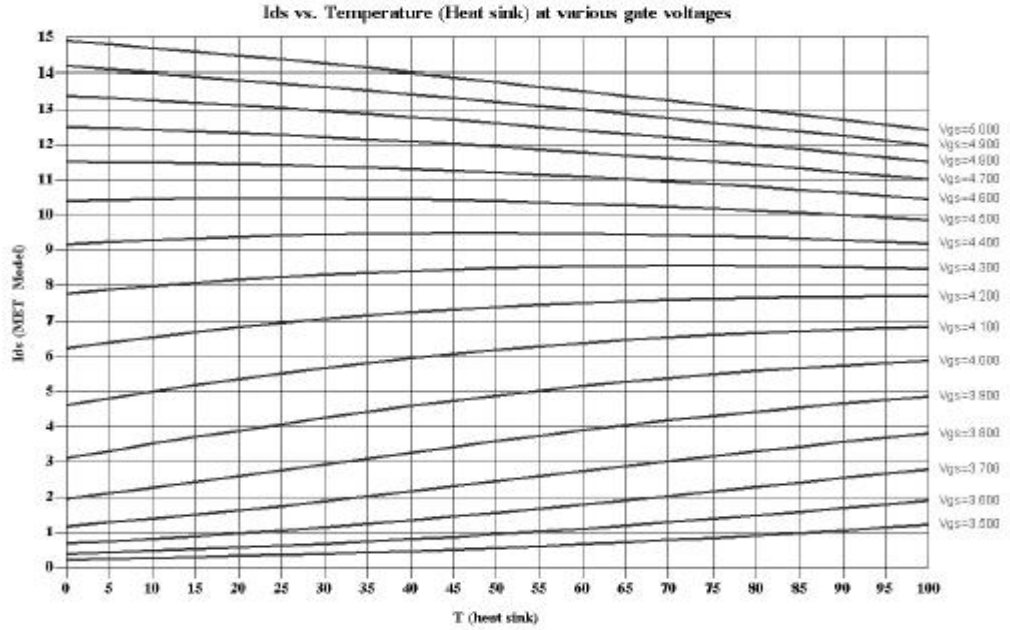
Sample Netlist:

```
.options f0 = 1.0e7 jupdm=4 output=0 temp=298.
.tran2 tstep=0.1ns tstop=10ns
MosnldMet:m1 2 3 0 1000 "tref"
res:rd 1 3 r=50
vsource:vds 1 0 vdc=26v
vsource:vgs 2 0 vdc=5v vac=1v f=1e9
vsource:t1 1000 "tref" vdc=temp
.ref "tref"
.out plot term 2 vt in "ldmos_tr.vgs"
```

```
.out plot term 3 vt in "ldmos_tr.vds"
.end
```

Validation:

The Validation of the model was done with transient, DC and thermal wave forms compared to the wave forms located in the Motorola LDMOS paper.



NOTE: For better viewing on the Web, click on link for larger version of graphic.

Figure 4. MET Model $T_{(heat\ sink)}$ Sweep Simulation at Constant V_{DS} and Parametric Values of V_{GS}

Figure 1: Ids vs. Temperature of the Motorola implemented LDMOS model

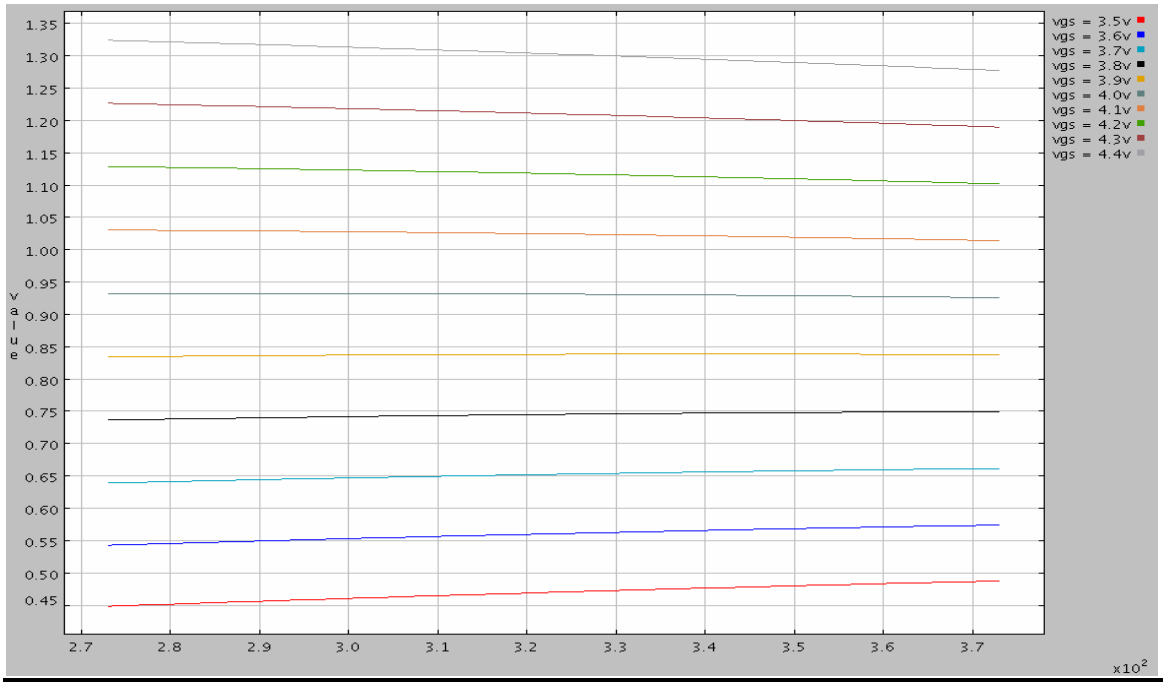
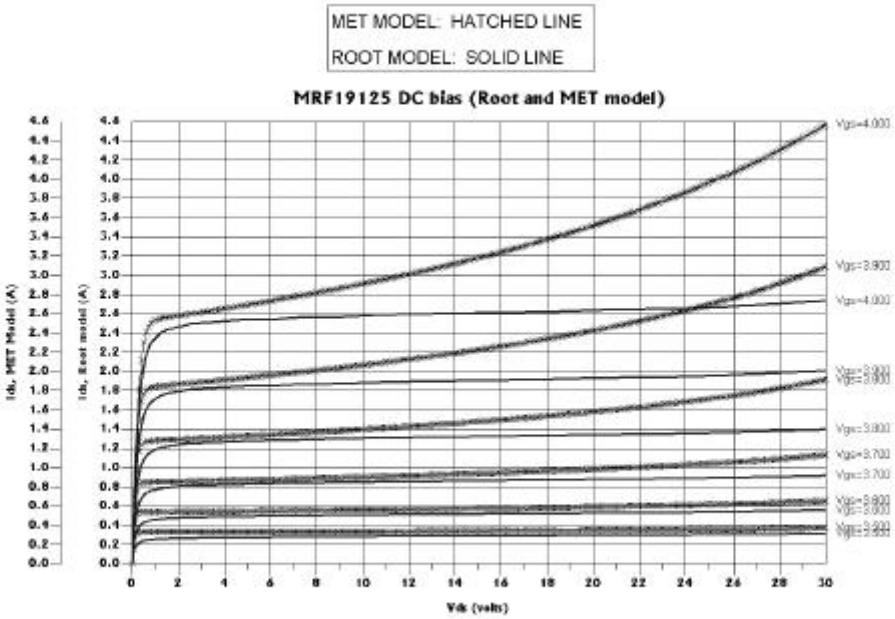


Figure 2: Ids vs. Temperature implemented in Freeda



NOTE: For better viewing on the Web of Step 4 graphic and Figure 5, click on link for larger versions of graphics.

Figure 5. Root and MET Model IV Curves Superimposed

Figure 3: Ids vs. Vds for the Motorola model for spice

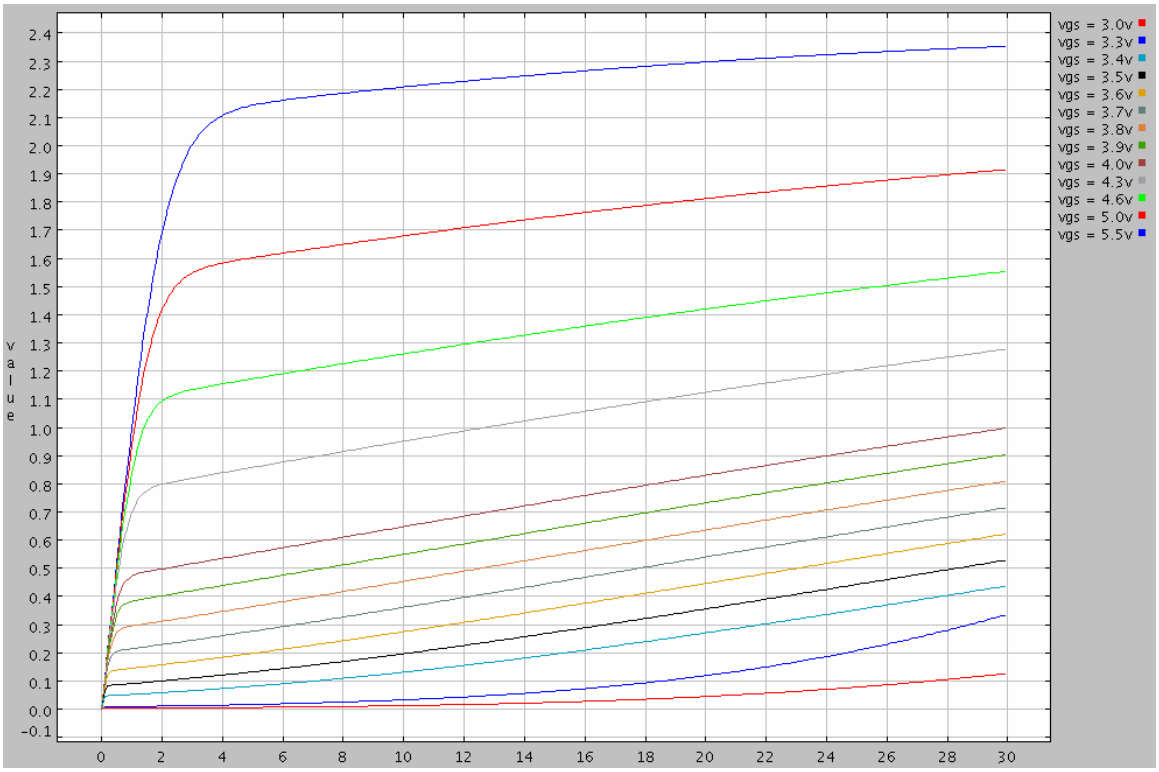


Figure 4: Ids vs. Vds for the LDMOS model in Freeda

Known Bugs:

The only difference between the Motorola model and this model is that in this model the Rdiode resistor has been left out. This is in series with the Idiode_r. It was seen to add to much complexity and after hand calculations did not cause much of a performance difference.

Version: 2003.05.15

Credits:

Name	Affiliation	Date	Links
Jiankai Chang		May 2003	
Jason Thurston		May 2003	