N Channel JFET jfetn

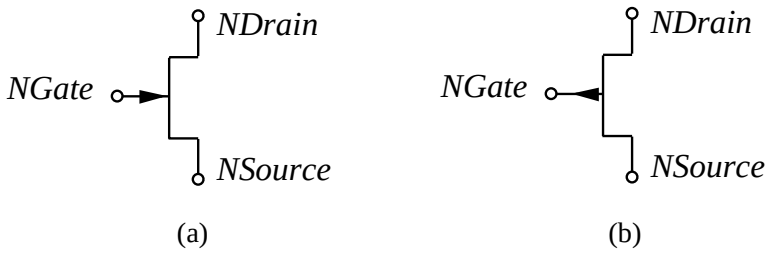

Figure 1: JFET Types (a) N-channel FET (b) P-channel FET

Form: `jfetn:`⟨`instance name`⟩ n_1 n_2 n_3 ⟨`parameter list`⟩
n_1 is the drain node,
n_2 is the gate node,
n_3 is the source node,
Parameters:

Parameter	Type	Default value	Required?
af: Flicker noise exponent	DOUBLE	1	no
area: Device area (m^2)	DOUBLE	1	no
beta: Transconductance parameter (A/V^2)	DOUBLE	0.0001	no
cgs: Zero bias gate source junction capacitance (F)	DOUBLE	0	no
cgd: Zero bias gate drain junction capacitance (F)	DOUBLE	0	no
eg: Barrier height at 0 K (eV)	DOUBLE	0.8	no
fc: Coefficient for forward bias depletion capacitance	DOUBLE	0.5	no
is: Gate junction saturation current (A)	DOUBLE	1×10^{-14}	no
kf: Flicker noise coefficient	DOUBLE	0	no
pb: Gate junction potential (1/V)	DOUBLE	0	no
rd: Drain ohmic resistance (ω)	DOUBLE	0	no
rs: Source ohmic resistance (ω)	DOUBLE	0	no
vt0: Threshold voltage (V)	DOUBLE	-2	no
m: Gate p-n grading coefficient	DOUBLE	0.5	no
vt0tc: Temperature coefficient for vt0 (V/K)	DOUBLE	0.0	no
tnom: Nominal temperature (K)	DOUBLE	300	no
b: Doping tail parameter	DOUBLE	1	no
t: Device temperature (K)	DOUBLE	300	no
lambda: Channel length modulation parameter (1/V)	DOUBLE	0	no

Example:

```
jfetn:j1 3 4 2 beta=0.0001
```

Description:
*f*REEDA™has the N-type JFET model based on the NJF model in SPICE.

DC Calculations:
Constants used are:

$$q = 1.6021918 \times 10^{-19}(As) \quad (1)$$
$$k = 1.3806226 \times 10^{-23}(J/K) \quad (2)$$

All parameters used are indicated in `this` font.

The current/voltage characteristics are evaluated after first determining the mode (normal: $V_{DS} \geq 0$ or inverted: $V_{DS} < 0$) and the region (cutoff, linear or saturation) of the current (V_{DS}, V_{GS}) operating point.

Normal Mode: ($V_{DS} \geq 0$)

Regions of operation:

$V_{GS} - V_{T0} \leq 0$	Cutoff Region
$0 \leq V_{DS} < V_{GS} - V_{T0}$	Linear Region
$0 < V_{GS} - V_{T0} \leq V_{DS}$	Saturation Region

Then

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ \texttt{AREA} \times \texttt{BETA}\,(1 + \texttt{LAMBDA}\,V_{DS})\,V_{DS}\,[2\,(V_{GS} - \texttt{VTO}) - V_{DS}] & \text{linear region} \\ \texttt{AREA} \times \texttt{BETA}\,(1 + \texttt{LAMBDA}\,V_{DS})\,(V_{GS} - \texttt{VTO})^2 & \text{saturation region} \end{cases} \quad (3)$$

Inverted Mode: ($V_{DS} < 0$)

Regions of operation:

$V_{GD} - V_{T0} \leq 0$	Cutoff Region
$0 \leq -V_{DS} < V_{GD} - V_{T0}$	Linear Region
$0 < V_{GD} - V_{T0} \leq -V_{DS}$	Saturation Region

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ \texttt{AREA} \times \texttt{BETA}\,(1 - \texttt{LAMBDA}V_{DS})\,V_{DS}\,[2\,(V_{GD} - \texttt{VTO}) + V_{DS}] & \text{linear region} \\ \texttt{AREA} \times\,(-\texttt{BETA})\,(1 - \texttt{LAMBDA}V_{DS})\,(V_{GD} - \texttt{VTO})^2 & \text{saturation region} \end{cases} \quad (4)$$

Leakage Currents
Current flows across the normally reverse biased source-bulk and drain-bulk junctions. The gate-source leakage current

$$I_{GS} = \texttt{AREA} \times\, I_S\, e^{(V_{GS}/\texttt{VTO} - 1)} \quad (5)$$

and the gate-source leakage current

$$I_{GD} = \texttt{AREA} \times\, I_S\, e^{(V_{GD}/\texttt{VTO} - 1)} \quad (6)$$

Capacitances
The drain-source capacitance

$$C_{DS} = \texttt{AREA} \times \texttt{CDS} \quad (7)$$

The gate-source capacitance

$$C_{GS} = \begin{cases} \texttt{AREA} \times \texttt{CGS}\left(1 - \frac{V_{GS}}{\texttt{PB}}\right)^{-\texttt{M}} & V_{GS} \leq \texttt{FC} \times \texttt{PB} \\ \texttt{AREA} \times \texttt{CGS}\,(1 - \texttt{FC})^{-(1+\texttt{M})}\left[1 - \texttt{FC}(1 + \texttt{M}) + \texttt{M}\frac{V_{GS}}{\texttt{PB}}\right]^{-\texttt{M}} & V_{GS} > \texttt{FC} \times \texttt{PB} \end{cases} \quad (8)$$

models charge storage at the gate-source depletion layer. The gate-drain capacitance

$$C_{GD} = \begin{cases} \texttt{AREA} \times \texttt{CGD}\left(1 - \frac{V_{GD}}{\texttt{PB}}\right)^{-\texttt{M}} & V_{GD} \leq \texttt{FC} \times \texttt{PB} \\ \texttt{AREA} \times \texttt{CGD}\,(1-\texttt{FC})^{-(1+\texttt{M})}\left[1 - \texttt{FC}(1+\texttt{M}) + \texttt{M}\frac{V_{GD}}{\texttt{PB}}\right]^{-\texttt{M}} & V_{GD} > \texttt{FC} \times \texttt{PB} \end{cases} \tag{9}$$

models charge storage at the gate-drain depletion layer.

Notes:
This is the J element in the SPICE compatible netlist.

Version:
2001.05.15

Credits:

Name	Affiliation	Date	Links
Nikhil Kriplani	NC State University	May 2001	NC STATE UNIVERSITY
nmkripla@unity.ncsu.edu			www.ncsu.edu
Shubha Vijaychand	NC State University	May 2001	NC STATE UNIVERSITY
svijayc@unity.ncsu.edu			www.ncsu.edu