0.0.1 MOSFET M

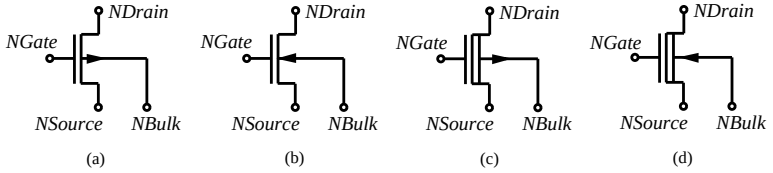

Figure 1: M — MOSFET element: (a) *n*-channel enhancement-mode MOSFET; (b) *p*-channel enhancement-mode MOSFET; (c) *n*-channel depletion-mode MOSFET; and (d) *p*-channel depletion-mode MOSFET.

Form:
`M`*name NDrain NGate NSsource NBulk ModelName* [`L=`*Length*] [`W=`*Width*]
`+` [`AD=`*DrainDiffusionArea*] [`AS=`*SourceDiffusionArea*]
`+` [`PD=`*DrainPerimeter*] [`PS=`*SourcePerimeter*]
`+` [`NRD=`*RelativeDrainResistivity*] [`NRS=`*RelativeSourceResistivity*]
`+` [`OFF`] [`IC=`V_{DS}, V_{GS}, V_{BS}]
where

NDrain is the drain node.

NGate is the gate node.

NSource is the source node.

NBulk is the bulk or substrate node.

ModelName is the model name.

L is the channel lateral diffusion *Length*.
(Units: m; Optional; Symbol: L; The default is version dependent.
Spice2g6 and Spice3 Default: the length `DEFL` most recently specified in a `.OPTION` statement which in-turn defaults to 100 μm (100U); PSpice Default: the length `L` – length specified in model *ModelName* which in turn defaults to the default length `DEFL` most recently specified in a `.OPTION` statement which in-turn defaults to 100 μm (100U).)

W is the channel lateral diffusion *Width*.
(Units: m; Optional; Symbol: W; The default is version dependent.
Spice2g6 and Spice3 Default: the width `DEFW` most recently specified in a `.OPTION` statement which in-turn defaults to 100 μm (100U);
PSpice Default: the width `W` – width specified in model *ModelName* which

in turn defaults to the default width DEFW most recently specified in a .OPTION statement which in-turn defaults to 100 μm (100U).)

AD is the area of the drain diffusion (*DrainDiffusionArea*). The default is DEFAD most recently specified in a .OPTIONS statement.
(Units: m^2; Optional; Default: DEFAD; Symbol: A_D)

AS is the area of the source diffusion (*SourceDiffusionArea*). The default is DEFAS most recently specified in a .OPTIONS statement.
(Units: m^2; Optional; Default: DEFAS; Symbol: A_S)

PD is the perimeter of the drain junction (*DrainPerimeter*).
(Units: m; Optional; Default: 0; Symbol: P_D)

PS is the perimeter of the source junction (*SourcePerimeter*).
(Units: m; Optional; Default: 0; symbol: P_S)

NRD is the relative resistivity in squares of the drain region (*RelativeDrainResistivity*). The sheet resistance RSH specified in the model *ModelName* is divided by this factor to obtain the parasitic drain resistance.
(Units: squares; Optional; Default: 0; Symbol: N_{RD})

NRS is the relative resistivity in squares of the source region (*RelativeSourceResistivity*). The sheet resistance RSH specified in the model *ModelName* is divided by this factor to obtain the parasitic source resistance.
(Units: squares; Optional; Default: 0; Symbol: N_{RS})

NRG is the relative resistivity in squares of the gate region (*RelativeGateResistivity*). The sheet resistance RSH specified in the model *ModelName* is divided by this factor to obtain the parasitic gate resistance.
(Units: squares; Optional; Default: 0; Symbol: N_{RG})

NRB is the relative resistivity in squares of the bulk (substrate) region (*RelativeBulkResistivity*). The sheet resistance RSH specified in the model *ModelName* is divided by this factor to obtain the parasitic bulk resistance.
(Units: squares; Optional; Default: 0; Symbol: N_{RB})

OFF indicates an (optional) initial condition on the device for DC analysis. If specified the DC operating point is calculated with the terminal voltages set to zero. Once convergence is obtained, the program continues to iterate to obtain the exact value of the terminal voltages. The OFF option is used to enforce the solution to correspond to a desired state if the circuit has more than one stable state.

IC is the optional initial condition specification. Using IC=V_{DS}, V_{GS}, V_{BS} is intended for use with the UIC option on the .TRAN line, when a transient analysis is desired starting from other than the quiescent operating point. Specification of the transient initial conditions using the .IC statement is

preferred and is more convenient.

Example:

```
M1 24 2 0 20 TYPE1
M31 2 17 6 10 MODM L=5U W=2U
M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U
```

Description:

The parameters of a MOSFET can be completely specified in the model *ModelName*. This facilitates the use of standard transistors by using absolute quantities in the model. Alternatively scalable process parameters can be specified in the model *ModelName* and these scaled by geometric parameters on the MOSFET element line. In SPICE2G6 and SPICE3 the width `W` can not be specified in the model statement. For these simulators absolute device parameters must be specified in the model statement if parameters are not input on the element line.

Model Type

```
NMOS
PMOS
```

Example

```
M1 5 5 1 1 PCH L=2.0U W=20U AD=136P AS=136P
.
.
.
.MODEL PCH PMOS LEVEL=2 VTO=-0.76 GAMMA=0.6 CGSO=3.35E-10
+ CGDO=3.35E-10 CJ=4.75E-4 MJ=0.4 TOX=225E-10 NSUB=1.6E16
+ XJ=0.2E-6 LD=0 UO=139 UEXP=0 KF=5E-30 LAMBDA=0.02
```

NMOS Model — N-CHANNEL MOSFET MODEL

PMOS Model — P-CHANNEL MOSFET MODEL

Two groups of model parameters define the linear and nonlinear elements of the MOSFET models. One group defines absolute quantities and another group defines quantities that are multiplied by scaling parameters related to area and dimension which are specified on the element line. This enables the MOSFET element to be used in two ways. Using the absolute quantities the characteristics of a device can be defined independent of the parameters on the element line. Thus the model of a standard transistor, perhaps resident in a library, can be used without user-knowledge required. Using the scalable quantities the parameters of a fabrication process can be defined in the model statement and scaling parameters such as the lateral diffusion length (specified by `L`) and the lateral diffusion width (specified by `W`), and the drain and source diffusion areas (specfified by `AD` and `AS` specified on the element line). An example is the specification of the drain-bulk saturation current $I_{D,\mathrm{SAT}}$. This parameter can be specified by the absolute parameter I_S specified by the `IS` model keyword. It can also be determined as $I_S = J_S \cdot A_D$ using the scalable parameter J_S specified by the `JS` model keyword and A_D specified by the `AD` element keyword.

Spice provides four MOSFET device models. The first three models, known as `LEVEL`s 1, 2 and 3 differ in the formulation of the I-V characteristic. The fourth model, known as the BSIM model, uses a completely different formulation utilizing extensive semiconductor parameters. The parameter `LEVEL` specifies the model to be used:

LEVEL = 1 → "Shichman-Hodges", MOS1
This model was the first SPICE MOSFET model and was developed in 1968 [**?**]. It is an elementary model and has a limited scaling capability. It is applicable to fairly large devices with gate lengths greater than 4 μm. Its main attribute is that only a few parameters need be specified and so it is good for preliminary analyses.

LEVEL = 2 → MOS2
This is an analytical model which uses a combination of processing parameters and geometry. The major development over the `LEVEL` 1 model is improved treatment of the capacitances due to the channel charge. [**?**, **?**, **?**]. The model dates from 1980 and is applicable for chanel lengths of 2 μm and higher [**?**].
The `LEVEL` 2 model has convergence problems and is slower and less accurate than the `LEVEL` 3 model.

LEVEL = 3 → MOS3
This is a semi-empirical model developed in 1980 [**?**]. It is also used for gate lengths of 2 μm and more. The parameters of this model are determined by experimental characterization and so it is more accurate than the `LEVEL` 1 and 2 models that use the more indirect process parameters.

LEVEL = 4 → BSIM or BSIM1
The BSIM model is an advanced empirical model which uses process information and a larger number of parameters (more than 60) to describe the operation of devices with gate lengths as short as 1 μm. It was developed in 1985 [**?**].

Other MOSFET models or `LEVEL`s are available in various versions of SPICE. These `LEVEL`s are optimized for MOSFETs fabricated in a particular foundary or provide a proprietary edge for the advanced commercial SPICE programs. The reader interested in more advanced MOSFET models is refered to [**?**].

LEVEL 1, 2 and 3 MOSFET models.

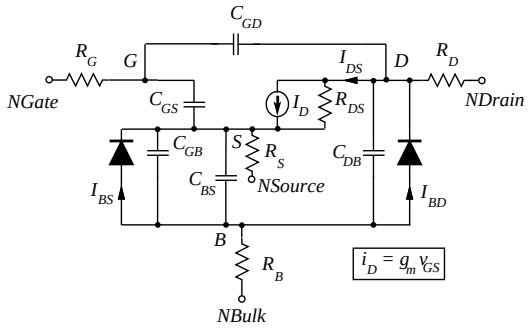

Figure 2: Schematic of `LEVEL` 1, 2 and 3 MOSFET models. V_{GS}, V_{DS}, V_{GD}, V_{GB}, V_{DB} and V_{BS} are voltages between the internal gate, drain, bulk and source terminals designated G, D, B and C respectively.

The LEVEL 1, 2 and 3 models have much in common. These models evaluate the junction depletion capacitances and parasitic resistances of a transistor in the same way. They differ in the procedure used to evaluate the overlap capacitances (C_{GD}, C_{GS} and C_{GB}) and that used to determine the current-voltage characteristics of the active region of a transistor. The overlap capacitances model charge storage as nonlinear thin-oxide capacitance distributed among the gate, source drain and bulk regions. These capacitances are important in describing the operation of MOSFETs. The `LEVEL` 1, 2 and 3 models are intimately intertwined as combinations of parameters can result in using equations from more than one model. The `LEVEL` parameter resolves conflicts when there is more than one way to calculate the transistor characteristics with the parameters specified by the user. Antognetti and Massobrio provide a comprehensive discussion of the development of the `LEVEL` 1, 2 and 3 models [**?**].

The parameters of the `LEVEL` 1, 2 and 3 models are given in table 1. Parameter extensions for PSpice are given in table 4. It is assumed that the model parameters were determined or measured at the nominal temperature $T_{\rm NOM}$ (default $27°C$) specified in the most recent `.OPTIONS` statement preceeding the `.MODEL` statement. In PSpice this is overwritten by the `T_MEASURED` parameter. Most of the parameters have default values. Those parameters that have INFERRED defaults are calculated from other parameters.

The MOSFET `LEVEL` 1,2 and 3 parameters fall into three categories: absolute device parameters, scalable and process parameters and geometric parameters. In most cases the absolute device parameters can be derived from the scalable and process parameters and the geometry parameters. However, if specified, the values of the device parameters are used.

Table 1: MOSFET model keywords for LEVELs 1, 2, 3.

Name	Description	Units	Default
AF	flicker noise exponent (A_F)	-	1
CBD	zero-bias B-D junction capacitance (C'_{BD})	F	0
CBS	zero-bias B-S junction capacitance (C'_{BS})	F	0
CGBO	gate-bulk overlap capacitance per meter of channel length (PARASITIC) (C_{GBO})	F/m	0
CGDO	gate-drain overlap capacitance per meter of channel width (PARASITIC) (C_{GDO})	F/m	0
CGSO	gate-source overlap capacitance per meter of channel width (PARASITIC) (C_{GSO})	F/m	0
CJ	zero-bias bulk junction bottom capcitance per square meter of junction area (PARASITIC) (C_J)	F/m^2	0
CJSW	zero-bias bulk junction sidewall capacitance per meter of junction perimeter (PARASITIC) ($C_{J,SW}$)	F/m	0
DELTA	width effect on threshold voltage (LEVEL=2 and LEVEL=3) (δ)	-	0
ETA	static feedback (LEVEL=3 only) (η)	-	INFERRED

The physical constants used in the model evaluation are

k	Boltzmann's constant	$1.3806226\,10^{-23}$ J/K
q	electronic charge	$1.6021918\,10^{-19}$ C
ϵ_0	free space permittivity	$8.854214871\,10^{-12}$ F/m
$\epsilon_{\rm Si}$	permittivity of silicon	$11.7\epsilon_0$
$\epsilon_{\rm OX}$	permittivity of silicon dioxide	$3.9\epsilon_0$
n_i	intrinsic concentration of silicon @ 300 K	$1.45\,10^{16}$ m^{-3}

Standard Calculations

Absolute temperatures (in kelvins, K) are used. The thermal voltage

$$V_{\mathrm{TH}}(T_{\mathrm{NOM}}) = \frac{kT_{\mathrm{NOM}}}{q}. \tag{1}$$

The silicon bandgap energy

$$E_G(T_{\mathrm{NOM}}) = 1.16 - 0.000702\frac{4T_{\mathrm{NOM}}^2}{T_{\mathrm{NOM}} + 1108}. \tag{2}$$

The difference of the gate and bulk contact potentials

$$\phi_{\mathrm{MS}} = \phi_{\mathrm{GATE}} - \phi_{\mathrm{BULK}}. \tag{3}$$

The gate contact potential

$$\phi_{\mathrm{GATE}} = \begin{cases} 3.2 & T_{\mathrm{PG}} = 0 \\ 3.25 & \text{NMOS \& } T_{\mathrm{PG}} = 1 \\ 3.25 + E_G & \text{NMOS \& } T_{\mathrm{PG}} = -1 \\ 3.25 + E_G & \text{PMOS \& } T_{\mathrm{PG}} = 1 \\ 3.25 & \text{PMOS \& } T_{\mathrm{PG}} = -1 \end{cases}. \tag{4}$$

The potential drop across the oxide

$$\phi_{\mathrm{OX}} = -\frac{Q'_0}{C'_{\mathrm{OX}}}. \tag{5}$$

The contact potential of the bulk material

$$\phi_{\mathrm{BULK}} = \begin{cases} 3.25 + E_G & \text{if NMOS} \\ 3.25 & \text{if PMOS} \end{cases}. \tag{6}$$

The equivalent gate oxide interface charge per unit area

$$Q'_0 = qN_{\mathrm{SS}}. \tag{7}$$

The capacitance per unit area of the oxide is

$$C'_{OX} = \frac{\epsilon_{OX}}{T_{OX}}. \tag{8}$$

The effective length L_{EFF} of the channel is reduced by the amount X_{JL} (= `LD`) of the lateral diffusion at the source and drain regions:

$$L_{\mathrm{EFF}} = L - 2X_{JL} \tag{9}$$

Similarly the effective length W_{EFF} of the channel is reduced by the amount W_D (= `WD`) of the lateral diffusion at the edges of the channel.

$$W_{\mathrm{EFF}} = W - 2W_D \tag{10}$$

κ is limited: if the specified value of κ is less than or equal to zero the following parameters are set:

$$\kappa = 0.2 \tag{11}$$
$$\lambda = 0 \tag{12}$$
$$U_C = 0 \tag{13}$$
$$U_{\mathrm{EXP}} = 0 \tag{14}$$
$$U_{\mathrm{TRA}} = 0 \tag{15}$$

Process Oriented Model

If omitted, device parameters are computed from process parameters using defaults if necessary provided that both TOX $= T_{OX}$ and NSUB $= N_B$ are specified. If either TOX or NSUB is not specified then the critical device parameters must be specified. Which parameters are critical depends on the model LEVEL.

If VTO is not specified in the model statement then it is evaluated as

$$\texttt{VTO} = V_{T0} = \begin{cases} V_{\rm FB} + \gamma\sqrt{2\phi_B} + 2\phi_B & \text{if NMOS} \\ V_{\rm FB} - \gamma\sqrt{2\phi_B} + 2\phi_B & \text{if PMOS} \end{cases} \tag{16}$$

where

$$V_{\rm FB} = \phi_{\rm MS} - \phi_{\rm OX} \tag{17}$$

is the flat-band voltage. Otherwise if VTO is specified in the model statement

$$V_{\rm FB} = \begin{cases} V_{T0} - \gamma\sqrt{2\phi_B} + 2\phi_B & \text{if NMOS} \\ V_{T0} + \gamma\sqrt{2\phi_B} + 2\phi_B & \text{if PMOS} \end{cases} \tag{18}$$

If GAMMA is not specified in the model statement then

$$\texttt{GAMMA} = \gamma = \frac{\sqrt{2\epsilon_{\rm Si} q N_B}}{C'_{OX}} \tag{19}$$

If PHI is not specified in the model statement then

$$\texttt{PHI} = 2\phi_B = 2V_{\rm TH} \ln \frac{N_B}{n_i} \tag{20}$$

and is limited to 0.1 if calculated. $N_B =$ NSUB as supplied in the model statement and n_i at 300 K are used. If KP is not specified in the model statement then

$$\texttt{KP} = K_P = \mu_0 C'_{OX} \tag{21}$$

If UCRIT is not specified in the model statement then

$$\texttt{UCRIT} = U_C = \frac{\epsilon_{Si}}{T_{OX}} \tag{22}$$

$$X_d = \sqrt{\frac{2\epsilon_{\rm Si}}{qN_B}} \tag{23}$$

is proportional to the depletion layer widths at the source and rdain regions.

Temperature Dependence

Temperature effects are incorporated as follows where T and $T_{\rm NOM}$ are absolute temperatures in Kelvins (K).

$$V_{\rm TH} = \frac{kT}{q} \tag{24}$$

$$I_S(T) = I_S e^{\left(E_g(T)\frac{T}{T_{\rm NOM}} - E_G(T)\right)/V_{\rm TH}} \tag{25}$$

$$J_S(T) = J_S e^{\left(E_g(T)\frac{T}{T_{\rm NOM}} - E_G(T)\right)/V_{\rm TH}} \tag{26}$$

$$J_{S,\rm SW}(T) = J_{S,\rm SW} e^{\left(E_g(T)\frac{T}{T_{\rm NOM}} - E_G(T)\right)/V_{\rm TH}} \tag{27}$$

$$\phi_J(T) = \phi_J \frac{T}{T_{\rm NOM}} - 3V_{\rm TH}\ln\frac{T}{T_{\rm NOM}} + E_G(T_{\rm NOM})\frac{T}{T_{\rm NOM}} - E_G(T) \tag{28}$$

$$\phi_{J,\rm SW}(T) = \phi_{J,\rm SW} \frac{T}{T_{\rm NOM}} - 3V_{\rm TH}\ln\frac{T}{T_{\rm NOM}} + E_G(T_{\rm NOM})\frac{T}{T_{\rm NOM}} - E_G(T) \tag{29}$$

$$2\phi_B(T) = 2\phi_B \frac{T}{T_{\rm NOM}} - 3V_{\rm TH}\ln\frac{T}{T_{\rm NOM}} + E_G(T_{\rm NOM} - E_G(T) \tag{30}$$

$$C'_{BD}(T) = C'_{BD}\{1 + M_J[0.0004(T - T_{\rm NOM}) + (1 - \phi_J(T)/\phi_J)]\} \tag{31}$$

$$C'_{BS}(T) = C'_{BS}\{1 + M_J[0.0004(T - T_{\rm NOM}) + (1 - \phi_J(T)/\phi_J)]\} \tag{32}$$

$$C_J(T) = C_J\{1 + M_J[0.0004(T - T_{\rm NOM}) + (1 - \phi_{J,\rm SW}(T)/\phi_{J,\rm SW})]\} \tag{33}$$

$$C_{J,\rm SW}(T) = C_{J,\rm SW}\{1 + M_{J,\rm SW}[0.0004(T - T_{\rm NOM}) + (1 - \phi_J(T)/\phi_J)]\} \tag{34}$$

$$K_P(T) = K_P(T_{\rm NOM}/T)^{3/2} \tag{35}$$

$$\mu_0(T) = \mu_0(T_{\rm NOM}/T)^{3/2} \tag{36}$$

$$E_g(T) = 1.16 - 0.000702\frac{T^2}{T + 1108} \tag{37}$$

$$\tag{38}$$

<u>*Parasitic Resistances*</u>

The resistive parasitics R_S, R_G, R_D and R_B are treated in the same way for the `LEVEL` 1, 2 and 3 models. They may be specified as the absolute device parameters `RS`, `RG`, `RD`, and `RB` or calculated from the sheet resistivity $R_{\rm SH}$ (= `RSH`) and area parameters N_{RS} (= `NRS`), N_{RG} (= `NRG`), N_{RD} (= `NRD`) and N_{RB} (= `NRB`). As always the absolute device parameters take precedence if they are specified. Otherwise

$$R_S = N_{RS} R_{\rm SH} \tag{39}$$
$$R_G = N_{RG} R_{\rm SH} \tag{40}$$
$$R_D = N_{RD} R_{\rm SH} \tag{41}$$
$$R_B = N_{RB} R_{\rm SH} \tag{42}$$

Note that neither geometry parameters nor process parameters are required if the absolute device resistances are specified. The parasitic resistance parameter dependencies are summarized in figure 3. *Leakage Currents*

Current flows across the normally reverse biased source-bulk and drain-bulk junctions. The bulk-source leakage current

$$I_{BS} = I_{BSS}\left(e^{(V_{BS}/V_{\rm TH})} - 1\right) \tag{43}$$

where

$$I_{BSS} = \begin{cases} I_S & \text{if } \texttt{IS} \text{ specified} \\ A_S J_S + P_S J_{S,\rm SW} & \text{if } \texttt{IS} \text{ not specified} \end{cases} \tag{44}$$

The bulk-drain leakage current

$$I_{BD} = I_{BDS}\left(e^{(V_{BD}/V_{\rm TH})} - 1\right) \tag{45}$$

where

$$I_{BDS} = \begin{cases} I_S & \text{if } \texttt{IS} \text{ specified} \\ A_D J_S + P_S J_{S,\rm SW} & \text{if } \texttt{IS} \text{ not specified} \end{cases} \tag{46}$$

The parameter dependencies of the parameters describing the leakage current in the `LEVEL` 1, 2 and 3 MOSFET models are summarized in figure 4.

PROCESS PARAMETERS	
`RSH`	$R_{\rm SH}$

+

GEOMETRY PARAMETERS	
`NRS`	N_{RS}
`NRD`	N_{RD}
`NRG`	N_{RG}
`NRB`	N_{RB}

→

DEVICE PARAMETERS	
`RD`	$R_D = f(R_{\rm SH}, N_{RD})$
`RS`	$R_S = f(R_{\rm SH}, N_{RS})$
`RG`	$R_B = f(R_{\rm SH}, N_{RG})$
`RB`	$R_B = f(R_{\rm SH}, N_{RB})$

Figure 3: MOSFET `LEVEL` 1, 2 and 3 parasitic resistance parameter relationships.

Depletion Capacitances

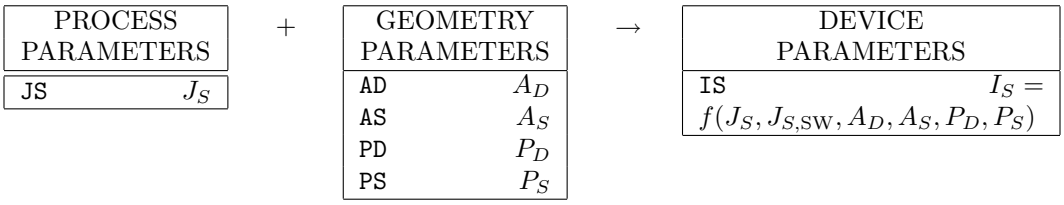

Figure 4: MOSFET leakage current parameter dependecies.

C_{BS} and C_{BD} are the depletion capacitances at the bulk-source and bulk-drain depletion regions respectively. These depletion capacitances are calculated and used in the same way in all three (`LEVEL` = 1, 2 and 3) models. Although they may be specified as absolute device parameters they are strong functions of the voltages across the junction and are complex functions of geometry and of semiconductor doping. As such they are usually calculated from process parameters. They are the sum of component capacitances

$$C_{BS} = C_{BS,\mathrm{JA}} + C_{BS,\mathrm{SW}} + C_{BS,\mathrm{TT}} \tag{47}$$

where the sidewall capacitance

$$C_{BS,\mathrm{SW}} = P_S C_{J,\mathrm{SW}} C_{BSS} \tag{48}$$

$$C_{BSS} = \begin{cases} \left(1 - \frac{V_{BS}}{\phi_{J,\mathrm{SW}}}\right)^{-M_{J,\mathrm{SW}}} & \text{for } V_{BS} \le F_C \phi_J \\ (1-F_C)^{-(1+M_{J,\mathrm{SW}})} \left(1 - F_C(1+M_{J,\mathrm{SW}}) + \frac{M_{J,\mathrm{SW}} V_{BS}}{\phi_{J,\mathrm{SW}}}\right) & \text{for } V_{BS} > F_C \phi_J \end{cases} \tag{49}$$

(50)

the area capacitance

$$C_{BS,\mathrm{JA}} = \begin{cases} C'_{BS} C_{BSJ} & \text{if } \texttt{CBS}\ (= C'_{BS}) \text{ is specified in the model} \\ A_S C_J C_{BSJ} & \text{otherwise} \end{cases} \tag{51}$$

$$C_{BSJ} = \begin{cases} \left(1 - \frac{V_{BS}}{\phi_J}\right)^{-M_J} & \text{for } V_{BS} \le F_C \phi_J \\ (1-F_C)^{-(1+M_J)} \left(1 - F_C(1+M_J) + \frac{M_J V_{BS}}{\phi_J}\right) & \text{for } V_{BS} > F_C \phi_J \end{cases} \tag{52}$$

and the transit time capacitance

$$C_{BS,\mathrm{TT}} = \tau_T G_{BS} \tag{53}$$

where the bulk-source conductance $G_{BS} = \partial I_{BS}/\partial V_{BS}$ and I_{BS} is defined in (43).

$$C_{BD} = C_{BD,\mathrm{JA}} + C_{BD,\mathrm{SW}} \tag{54}$$

where the sidewall capacitance

$$C_{BD,\mathrm{SW}} = P_D C_{J,\mathrm{SW}} C_{BDS} \tag{55}$$

$$C_{BDS} = \begin{cases} \left(1 - \frac{V_{BD}}{\phi_{J,\mathrm{SW}}}\right)^{-M_{J,\mathrm{SW}}} & \text{for } V_{BD} \le F_C \phi_J \\ (1-F_C)^{-(1+M_{J,\mathrm{SW}})} \left(1 - F_C(1+M_{J,\mathrm{SW}}) + \frac{M_{J,\mathrm{SW}} V_{BD}}{\phi_{J,\mathrm{SW}}}\right) & \text{for } V_{BD} > F_C \phi_J \end{cases} \tag{56}$$

(57)

the area capacitance

$$C_{BD,\mathrm{JA}} = \begin{cases} C'_{BD} C_{BDJ} & \text{if } \texttt{CBD}\ (= C'_{BD}) \text{ is specified in the model} \\ A_D C_J C_{BDJ} & \text{otherwise} \end{cases} \tag{58}$$

$$C_{BDJ} = \begin{cases} \left(1 - \frac{V_{BD}}{\phi_J}\right)^{-M_J} & \text{for } V_{BS} \le F_C \phi_J \\ (1-F_C)^{-(1+M_J)} \left(1 - F_C(1+M_J) + \frac{M_J V_{BD}}{\phi_J}\right) & \text{for } V_{BD} > F_C \phi_J \end{cases} \tag{59}$$

and the transit time capacitance

$$C_{BS,\mathrm{TT}} = \tau_T G_{BS} \tag{60}$$

where the bulk-source conductance $G_{BD} = \partial I_{BD}/\partial V_{BD}$ and I_{BD} is defined in (45).

In the LEVEL 1 MOSFET model the depletion capacitances are piecewise linear. They are calculated at the current operating point and then treated as linear. In the LEVEL 2 and 3 models they are treated as nonlinear. The depletion capacitance parameter dependencies are summarized in figure 5.

LEVEL 1 *I/V Characteristics*

For the LEVEL 1 model the device parameters (other than capacitances and resistances) are evaluated using T_{OX} (TOX), μ_0 (UO), $N_{\rm SS}$ (NSS and N_B (NSUB) if they are not specified in the .MODEL statement.

The LEVEL 1 current/voltage characteristics are evaluated after first determining the mode (normal: $V_{DS} \geq 0$ or inverted: $V_{DS} < 0$) and the region (cutoff, linear or saturation) of the current (V_{DS}, V_{GS}) operating point.

Normal Mode: ($V_{DS} \geq 0$)

The regions are as follows:

cutoff region:	$V_{GS} < V_T$
linear region:	$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$
saturation region:	$V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$

PROCESS PARAMETERS		+	GEOMETRY PARAMETERS		→	DEVICE PARAMETERS	
CJ	C_J		AD	A_D		CBD	$C'_{BD} = f(C_J, A_D)$
CJSW	$C_{J,\rm SW}$		AS	A_S		CBS	$C'_{BS} = f(C_J, A_S)$
MJ	M_J		PD	P_D		$\{C_{BS} = f(P_S, C'_{BS}, C_{J,\rm SW}, \tau_T$	
MJSW	$M_{J,\rm SW}$		PS	P_S		$M_J, M_{J,\rm SW}, \phi_J, \phi_{J,\rm SW}, F_C)\}$	
PB	ϕ_J					$\{C_{BD}$	$=$
PBSW	$\phi_{J,\rm SW}$					$f(P_D, C'_{BD}, C_{J,\rm SW}, \tau_T$	
FC	F_C					$M_J, M_{J,\rm SW}, \phi_J, \phi_{J,\rm SW}, F_C)\}$	

Figure 5: MOSFET LEVEL 1, 2 and 3 junction depletion capacitance parameter relationships.

where the threshold voltage

$$V_T = \begin{cases} V_{\rm FB} + 2\phi_B + \gamma\sqrt{2\phi_B - V_{BS}} & V_{BS} \geq 2\phi_B \\ V_{\rm FB} + 2\phi_B & V_{BS} < 2\phi_B \end{cases} \tag{61}$$

Then

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ \dfrac{W_{\rm EFF}}{L_{\rm EFF}} \dfrac{K_P}{2} (1 + \lambda V_{DS}) V_{DS} \left[2(V_{GS} - V_T) - V_{DS}\right] & \text{linear region} \\ \dfrac{W_{\rm EFF}}{L_{\rm EFF}} \dfrac{K_P}{2} (1 + \lambda V_{DS}) \left[V_{GS} - V_T\right]^2 & \text{saturation region} \end{cases} \tag{62}$$

Inverted Mode: ($V_{DS} < 0$)

In the inverted mode the MOSFET I/V characteristics are evaluated as in the normal mode (62) but with the drain and source subscripts interchanged. The relationships of the parameters describing the I/V characteristics for the `LEVEL` 1 model are summarized in figure 6.

PROCESS PARAMETERS	
`NSUB`	N_B
`TOX`	T_{OX}
`NSS`	$N_{\rm SS}$
`UO`	μ_0

+

GEOMETRY PARAMETERS	
–	
Required	
`L`	L
`W`	W
Optional	
`LD`	X_{JL}
`WD`	W_D

→

DEVICE PARAMETERS	
`VTO`	$V_{T0} = f(2\phi_B, N_{\rm SS}, T_{OX}, \gamma)$
`KP`	$K_P = f(\mu_0, T_{OX})$
`LAMBDA`	λ
`PHI`	$2\phi_B = f(N_B)$
`GAMMA`	$\gamma = f(T_{OX}, N_B)$
$\{I_D = f(W, L, W_D, X_{JL}$	$V_{T0}, K_P, \lambda, 2\phi_B, \gamma)\}$

Figure 6: LEVEL 1 I/V dependencies.

LEVEL *1 Overlap Capacitances*

. In the LEVEL 1 model the gate overlap capacitances C_{GS}, C_{GD} and C_{GB} are constant and are calculated using the per unit width overlap capacitances C_{GSO} (CGSO), C_{GDO} (CGDO) and C_{GBO} (CGBO):

$$C_{GS} = C_{GSO}W \quad (63)$$
$$C_{GD} = C_{GDO}W \quad (64)$$
$$C_{GB} = C_{GBO}W \quad (65)$$

The overlap capacitance parameter dependencies are summarized in figure 7.

LEVEL 2 *I/V Characteristics*

The LEVEL 2 I/V characteristics are based on empirical fits resulting in a more accurate description of the I/V response than obtained with the LEVEL 1 model. The LEVEL 2 current/voltage characteristics are evaluated after first determining the mode (normal: $V_{DS} \geq 0$ or inverted: $V_{DS} < 0$) and the region (cutoff, linear or saturation) of the current (V_{DS}, V_{GS}) operating point.

Normal Mode: ($V_{DS} \geq 0$)

The regions are as follows:

PROCESS PARAMETERS
–

+

GEOMETRY PARAMETERS	
Required	
W	W
Optional	
WD	W_D

→

DEVICE PARAMETERS	
Overlap Capacitances	
CGSO	C_{GSO}
CGDO	C_{GDO}
CGBO	C_{GBO}
$\{C_{GS} = f(C_{GSO}, W, W_D)\}$	
$\{C_{GD} = f(C_{GDO}, W, W_D)\}$	
$\{C_{GB} = f(C_{GBO}, W, W_D)\}$	

Figure 7: MOSFET LEVEL 1 overlap capacitance parameter relationships.

cutoff region:	$V_{GS} < V_T$
weak inversion region:	$V_T < V_{GS} \leq V_{\rm ON}$
linear region (strong inversion):	$V_{GS} > V_{\rm ON}$ and $V_{DS} < V_{DS,\rm SAT}$
saturation region (strong inversion):	$V_{GS} > V_{\rm ON}$ and $V_{DS} > V_{DS,\rm SAT}$

where

$$V_T = V'_{\rm FB} + \gamma_{\rm EFF} X_S \tag{66}$$

$$V_{\rm ON} = \begin{cases} V_T & N_{\rm FS} = 0 \\ V_T + V_{\rm TH} x_n & N_{\rm FS} \neq 0 \end{cases} \tag{67}$$

$$X_S = \begin{cases} \dfrac{\sqrt{2\phi_B}}{[1 + \frac{1}{2} V_{BS}/(2\phi_B)]} & V_{BS} > 0 \\ \sqrt{2\phi_B - V_{BS}} & V_{BS} \leq 0 \end{cases} \tag{68}$$

where

$$x_n = 1 + F_N - \gamma_{\rm EFF} X_1 - X_2 X_S + W_{\rm EFF} L_{\rm EFF} \frac{q N_{\rm FS}}{C'_{OX}} \tag{69}$$

$$\eta = 1 + F_N \tag{70}$$

the effect of channel width on threshold voltage is modeled by

$$V'_{\rm FB} = V_{\rm FB} + F_N (2\phi_B - V_{BS}) \tag{71}$$

and the flat band voltage, $V_{\rm FB}$, is calculated using (17) or (18).

$$V_{GST} = V_{GS} - V_{ON} \tag{72}$$

The factor describing the effect of channel width on threshold is

$$F_N = \frac{\epsilon_s \delta \pi}{4 C'_{OX} W_{\rm EFF}} \tag{73}$$

The effective bulk threshold parameter is affected by charge in the drain and source depletion regions. This is important for short channels. The factor describing short channel effects is

$$\gamma_{\rm EFF} = \begin{cases} \gamma & \gamma \leq 0 \text{ or } N_B \leq 0 \\ \gamma(1 - F_{DD} - F_{SD}) & \gamma > 0 \text{ and } N_B > 0 \end{cases} \tag{74}$$

where the effect of depletion charge at the drain is described by

$$F_{DD} = \begin{cases} \frac{1}{2}\left(\sqrt{1 + 2X_D X_B} - 1\right) & V_{DS} \leq V_{DS,\rm SAT} \\ \frac{1}{2}\left(\sqrt{1 + 2X_D X_{B,\rm SAT}} - 1\right) \frac{X_J}{L_{\rm EFF}} & V_{DS} > V_{DS,\rm SAT} \end{cases} \tag{75}$$

the effect of depletion charge at the source is described by

$$F_{SD} = \frac{1}{2}\left(\sqrt{1 + 2X_D X_S} - 1\right) \frac{X_J}{L_{\rm EFF}} \tag{76}$$

and

$$X_B = \begin{cases} \dfrac{\sqrt{2\phi_B}}{[1 + \frac{1}{2}(V_{BS} - V_{DS})/(2\phi_B)]} & V_{DS} < V_{BS} \\ \sqrt{2\phi_B + V_{DS} - V_{BS}} & V_{DS} \leq V_{BS} \end{cases} \tag{77}$$

and for saturation

$$X_{B,\rm SAT} = \begin{cases} \dfrac{\sqrt{2\phi_B}}{[1 + \frac{1}{2}(V_{BS} - V_{DS,\rm SAT})/(2\phi_B)]} & V_{DS,\rm SAT} < V_{BS} \\ \sqrt{2\phi_B + V_{DS,\rm SAT} - V_{BS}} & V_{DS,\rm SAT} \geq V_{BS} \end{cases} \tag{78}$$

X_S is evaluated using (68) and X_D using (147).

$$X_1 = \begin{cases} \dfrac{-X_S^2}{2(2\phi_B)^{(3/2)}} & V_{BS} > 0 \\ -\dfrac{1}{2X_S} & V_{BS} \leq 0 \end{cases} \tag{79}$$

and

linear region

$$I_D = K_P \frac{W_{\rm EFF}}{L_{\rm EFF}} F_G F_D \left[\left(V_{GS} - V'_{\rm FB} - \frac{\eta}{2} V_{DS} \right) V_{DS} - \frac{3}{2} \frac{\gamma_{\rm EFF}}{\eta} F_B \right] \tag{101}$$

weak inversion region

When V_{GS} is slightly above V_T, I_D increases slowly over a few thermal voltages $V_{\rm TH}$ in exponential manner becoming I_D calculated for strong inversion. This effect is handled empirically by defining two exponential which, as well as ensuring an exponential increase in I_D, also ensure that the transconductance G_M $(= \partial I_D / \partial V_{GS})$ is continuous at $V_{GS} = V_{\rm ON}$.

$$I_D = \begin{cases} I_{D,\rm ON} \left[\frac{10}{11} e^{(V_{GS} - V_{\rm ON})/(x_n V_{TH})} + \frac{1}{11} e^{\alpha (V_{GS} - V_{\rm ON})} \right] & \alpha > 0 \\ I_{D,\rm ON} e^{(V_{GS} - V_{\rm ON})/(x_n V_{TH})} & \alpha \le 0 \end{cases} \tag{102}$$

where

$$\alpha = 11 \left(\frac{G_{M,\rm ON}}{I_{D,\rm ON}} - \frac{1}{x_n V_{\rm TH}} \right) \tag{103}$$

$$G_{M,\rm ON} = \frac{\partial I_{D,\rm ON}}{\partial V_{GS}} \tag{104}$$

$$I_{D,\rm ON} = \begin{cases} I_D \text{ in (101) with } V_{GS} = V_{ON} & V_{DS} \le V_{DS,\rm SAT} \\ I_D \text{ in (106) with } V_{GS} = V_{ON} \text{ and } V_{DS} = V_{DS,\rm SAT} & V_{DS} \le V_{DS,\rm SAT} \end{cases} \tag{105}$$

saturation region

$$I_D = \frac{L_{\rm EFF}}{L_{\rm EFF - \Delta_L}} I_{D,\rm SAT} \tag{106}$$

$$I_{D,\rm SAT} = K_P \frac{W_{\rm EFF}}{L_{\rm EFF}} F_G F_D \left[\left(V_{GS} - V'_{\rm FB} - \frac{\eta}{2} V_{DS,\rm SAT} \right) V_{DS,\rm SAT} - \frac{3}{2} \frac{\gamma_{\rm EFF}}{\eta} F_{B,\rm SAT} \right] \tag{107}$$

The `LEVEL` 3 current-voltage parameter dependencies are summarized in figure 8.

`LEVEL` *2 Overlap Capacitances*

In the `LEVEL 2` model the gate overlap capacitances asre strong functions of voltage. Two overlap capacitance models are available in PSpicethe Meyer model based on the model originally proposed by Meyer [**?**] and the Ward-Dutton model [**?**, **?**]. Spice2g6and Spice3use just the Meyer model. The Meyer and Ward-Dutton models differ in the derivation of the channel charge.

`LEVEL` *2 Meyer Model*

This model is selected when the parameter `XQC` $= X_{QC}$ is not specified or $X_{QC} < 0.5$.

The voltage dependent thin-oxide capacitances are used only if T_{OX} is specified in the model statement.

Four operating regions are defined in the Meyer model:

accumulation region:	$V_{GS} < V_{\rm ON} - 2\phi_B$
depletion region:	$V_{\rm ON} - 2\phi_B < V_{GS} < V_{\rm ON}$
saturation region:	$V_{\rm ON} < V_{GS} < V_{\rm ON} + V_{DS}$
linear region:	$V_{GS} > V_{\rm ON} + V_{DS}$

where

$$V_{\rm ON} = \begin{cases} V_T + x_n V_{\rm TH} & \text{if } N_{\rm FS} = \texttt{NFS} \text{ specified} \\ V_T & \text{if } N_{\rm FS} = \texttt{NFS} \text{ not specified} \end{cases} \tag{108}$$

$$V_T = V_{T0} + \gamma \left[\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B} \right] \tag{109}$$

$$x_n = 1 + \frac{qN_{\rm FS}}{C'_{OX}} + \frac{C_D}{C'_{OX}} \tag{110}$$

$$C'_{OX} = \frac{\epsilon_{OX}}{T_{OX}} \tag{111}$$

$$C_{OX} = C'_{OX} W_{\rm EFF} L_{\rm EFF} \tag{112}$$

$$C_D = \frac{\gamma}{2\sqrt{2\phi_B - V_{BS}}} \tag{113}$$

$$C_{GS} = \begin{cases} C_{GSO} W & \text{accumulation region} \\ \frac{2}{3} C_{OX} \left(1 + \frac{V_{\rm ON} - V_{GS}}{2\phi_B} \right) + C_{GSO} W_{\rm EFF} & \text{depletion region} \\ \frac{2}{3} C_{OX} + C_{GSO} W_{\rm EFF} & \text{saturation region} \\ C_{OX} \left\{ 1 - \left[\frac{V_{GS} - V_{DS} - V_{\rm ON}}{2(V_{GS} - V_{\rm ON}) - V_{DS}} \right]^2 \right\} + C_{GSO} W_{\rm EFF} & \text{linear region} \end{cases} \tag{114}$$

$$C_{GD} = \begin{cases} C_{GDO} W_{\rm EFF} & \text{accumulation region} \\ C_{GDO} W_{\rm EFF} & \text{depletion region} \\ C_{GDO} W_{\rm EFF} & \text{saturation region} \\ C_{OX} \left\{ 1 - \left[\frac{V_{GS} - V_{\rm ON}}{2(V_{GS} - V_{\rm ON}) - V_{DS}} \right]^2 \right\} + C_{GDO} W_{\rm EFF} & \text{linear region} \end{cases} \tag{115}$$

$$C_{GB} = \begin{cases} C_{OX} + C_{GBO} L_{\rm EFF} & \text{accumulation region} \\ C_{OX} \left(\frac{V_{\rm ON} - V_{GS}}{2\phi_B} \right) + C_{GBO} L_{\rm EFF} & \text{depletion region} \\ C_{GBO} L_{\rm EFF} & \text{saturation region} \\ C_{GBO} L_{\rm EFF} & \text{linear region} \end{cases} \tag{116}$$

LEVEL *2 Ward-Dutton Model* PSPICE *only*

This model is selected when the parameter `XQC` is specified and less than 0.5. The charge in the gate Q_G and the substrate Q_B is calculated and the difference of these is taken as the channel charge Q_{CHANNEL}. This charge is then partitioned and allocated between the source as Q_S and the drain Q_D as follows:

$$\begin{aligned} Q_{\text{CHANNEL}} &= Q_D + Q_S && (117)\\ Q_D &= X_{QC} Q_{\text{CHANNEL}} && (118)\\ & && (119) \end{aligned}$$

so that $Q_S = (1 - X_{QC})Q_{\text{CHANNEL}}$. This partitioning is somewhat arbitrary but produces transient results that more closely match measurements than does the Meyer capacitance model. However this is at the price of poorer convergence properties and sometimes error. This is particularly so when V_{DS} is changing sign.

Two operating regions are defined in the Ward-Dutton model:

off region: $V_{GS} \leq V_T$
on region: $V_{GS} > V_T$

where

$$\begin{aligned} V_T &= V_{T0} + \gamma \left[\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B} \right] && (120)\\ C_{OX} &= C'_{OX} W_{\text{EFF}} L_{\text{EFF}} && (121)\\ C'_{OX} &= \frac{\epsilon_{OX}}{T_{OX}} && (122)\\ & && (123) \end{aligned}$$

In the charge evaluations the following terms are used:

$$\begin{aligned} v_G &= v_{GB} - V'_{FB} + 2\phi_B && (124)\\ v_D &= \begin{cases} 2\phi_B - v_{BD} & v_{BD} > 2\phi_B \\ 0 & v_{BD} \leq 2\phi_B \end{cases} && (125)\\ v_S &= \begin{cases} 2\phi_B - v_{BS} & v_{BS} > 2\phi_B \\ 0 & v_{BS} \leq 2\phi_B \end{cases} && (126)\\ v_E &= \begin{cases} v_D & v_D < v_{DS,\text{SAT}} \\ v_{DS,\text{SAT}} & v_D \geq v_{DS,\text{SAT}} \end{cases} && (127)\\ x_5 &= (v_E + vs)(\sqrt{v_E} + \sqrt{v_S}) && (128)\\ x_6 &= ((v_E^2 + v_S^2) + v_E v_S) + \sqrt{v_E}\sqrt{v_S}(v_E + v_S) && (129)\\ D &= v_G(\sqrt{v_E} + \sqrt{v_S}) - \gamma_{\text{EFF}}((v_E + v_S) + \sqrt{v_E}\sqrt{v_S})/1.5 \\ & \quad -.5(\sqrt{v_E} + \sqrt{v_S})(v_E + v_S) && (130) \end{aligned}$$

where V'_{FB} is defined in (71) and $V_{DS,\text{SAT}}$ in (89).
off region

$$Q_G = \begin{cases} \gamma_{\rm EFF} C_{OX}(\sqrt{\frac{1}{4}\gamma_{\rm EFF}^2 + v_G} - \gamma_{\rm EFF}/2) & v_G > 0 \\ C_{OX} v_G & v_G \le 0 \end{cases} \quad (131)$$

$$Q_B = -Q_G \quad (132)$$

$$Q_{\rm CHANNEL} = -(Q_G + Q_B) \quad (133)$$

on region

$$Q_B = -\gamma_{\rm EFF} C_{OX} \left(\frac{vg\frac{2}{3}((v_E + v_S) + \sqrt{v_E}\sqrt{v_S}) - \frac{1}{2}\gamma_{\rm EFF} x_5 - .4x_6}{D} \right) \quad (134)$$

$$Q_G = C_{OX} \left(vg - \frac{.5vgx_5 - .4\gamma_{\rm EFF} x_6 - ((v_E^2 + v_S^2) + v_E v_S)(\sqrt{v_E} + \sqrt{v_S})/3}{D} \right) \quad (135)$$

where V'_{FB} is defined in (71). The overlap capacitances are then evaluated as

$$C_{GDB} = \partial Q_G / \partial v_D \quad (136)$$

$$C_{GSB} = \partial Q_G / \partial v_S \quad (137)$$

$$C_{GGB} = \partial Q_G / \partial v_G \quad (138)$$

$$C_{BDB} = \partial Q_B / \partial v_D \quad (139)$$

$$C_{BSB} = \partial Q_B / \partial v_S \quad (140)$$

$$C_{BGB} = \partial Q_B / \partial v_G \quad (141)$$

The `LEVEL` 2 overlap capacitance parameter dependencies are summarized in figure 9.

`LEVEL 3` *I/V Characteristics*

The `LEVEL` 3 I/V characteristics are based on empirical fits resulting in a more accurate description of the I/V response than obtained with the `LEVEL` 2 model. The `LEVEL 3` current/voltage characteristics are evaluated after first determining the mode (normal: $V_{DS} \ge 0$ or inverted: $V_{DS} < 0$) and the region (cutoff, linear or saturation) of the current (V_{DS}, V_{GS}) operating point.

Normal Mode: ($V_{DS} \ge 0$)

The regions are as follows:

cutoff region:	$V_{GS} < V_T$
weak inversion region:	$V_T < V_{GS} \leq V_{\rm ON}$
linear region (strong inversion):	$V_{GS} > V_{\rm ON}$ and $V_{DS} < V_{DS,\rm SAT}$
saturation region (strong inversion):	$V_{GS} > V_{\rm ON}$ and $V_{DS} > V_{DS,\rm SAT}$

where

$$V_T = V_{T0} - \sigma V_{DS} + F_C \tag{142}$$

the effect of short and narrow channel on threshold voltage

$$F_C = \gamma F_S \sqrt{2\phi_B - V_{BS}} + F_N(2\phi_B - V_{BS}) \tag{143}$$

and

$$V_{\rm ON} = \begin{cases} V_T & NFS = 0 \\ V_T + V_{TH} x_n & NFS \neq 0 \end{cases} \tag{144}$$

The effect of the short channel is described by

$$F_S = 1 - \frac{X_J}{L_{\rm EFF}} \left(\frac{X_{JL} + W_C}{X_J} \sqrt{1 - \frac{W_P}{X_J + W_P}} - \frac{X_{JL}}{X_J} \right) \tag{145}$$

where

$$W_P = X_D \sqrt{\phi_J - V_{BS}} \tag{146}$$

$$X_D = \sqrt{\frac{2\epsilon_s}{qN_B}} \tag{147}$$

$$W_C = X_J \left[0.0831353 + 0.8013929 \frac{W_P}{X_J} + 0.0111077 \frac{W_P}{X_J} \right] \tag{148}$$

and

$$\sigma = \eta \frac{8.15^{-22}}{C'_{OX} L^3_{\rm EFF}} \tag{149}$$

The effect of channel width on threshold is

$$F_N = \frac{\epsilon_s \delta \pi}{4 C'_{OX} W_{\rm EFF}} \tag{150}$$

The effective mobility due to modulation by the gate

$$\mu_S = \mu_0 F_G \tag{151}$$

and the factor describing mobility modulation by the gate is

$$F_G = \frac{1}{1 + \theta(V_{GSX} - V_T)} \tag{152}$$

where

$$V_{GSX} = \begin{cases} V_{GS} & V_{GS} < V_{\rm ON} \\ V_{\rm ON} & V_{GS} \geq V_{\rm ON} \end{cases} \tag{153}$$

The drain-source saturation voltage

$$V_{DS,\rm SAT} = \begin{cases} V_A + V_B - \sqrt{V_A^2 + V_B^2} & V_{\rm MAX} > 0 \\ V_P & V_{\rm MAX} \leq 0 \end{cases} \tag{154}$$

where

$$V_A = \frac{V_{GSX} - V_T}{1 + F_B} \tag{155}$$

$$V_B = \frac{v_{\rm MAX} L_{\rm EFF}}{\mu_S} \tag{156}$$

$$V_P = V_{GSX} - V_T \tag{157}$$

The body effect factor

$$F_B = \frac{\gamma F_S}{4\sqrt{\phi_{BS}}} + F_N \tag{158}$$

where

$$\phi_{BS} = \begin{cases} 2\phi_B - V_{BS} & V_{BS} \leq 0 \\ \dfrac{2\phi_B}{\sqrt{1 + \frac{1}{2} V_{BS}/(2\phi_B)}} & V_{BS} > 0 \end{cases} \tag{159}$$

The velocity saturation factor is

linear region

$$I_D = K_P \frac{W_{\text{EFF}}}{L_{\text{EFF}}} F_G F_D \left[V_{GSX} - V_T - \frac{1 + F_{\text{B}}}{2} V_{DS} \right] V_{DS} \tag{162}$$

weak inversion region

When V_{GS} is slightly above V_T, I_D increases slowly over a few thermal voltages V_{TH} in exponential manner becoming I_D calculated for strong inversion. This effect is handled empirically by defining two exponential which, as well as ensuring an exponential increase in I_D, also ensure that the transconductance G_M $(= \partial I_D / \partial V_{GS})$ is continuous at $V_{GS} = V_{\text{ON}}$.

$$I_D = \begin{cases} I_{D,\text{ON}} \left[\frac{10}{11} e^{(V_{GS} - V_{\text{ON}})/(x_n V_{TH})} + \frac{1}{11} e^{\alpha (V_{GS} - V_{\text{ON}})} \right] & \alpha > 0 \\ I_{D,\text{ON}} e^{(V_{GS} - V_{\text{ON}})/(x_n V_{TH})} & \alpha \leq 0 \end{cases} \tag{163}$$

where

$$\alpha = 11 \left(\frac{G_{M,\text{ON}}}{I_{D,\text{ON}}} - \frac{1}{x_n V_{\text{TH}}} \right) \tag{164}$$

$$G_{M,\text{ON}} = \frac{\partial I_{D,\text{ON}}}{\partial V_{GS}} \tag{165}$$

and

$$I_{D,\text{ON}} = \begin{cases} I_D \text{ in (162) with } V_{GS} = V_{ON} & V_{DS} \leq V_{DS,\text{SAT}} \\ I_D \text{ in (167) with } V_{GS} = V_{ON} \text{ and } V_{DS} = V_{DS,\text{SAT}} & V_{DS} \leq V_{DS,\text{SAT}} \end{cases} \tag{166}$$

saturation region

$$I_D = \frac{L_{\rm EFF}}{L_{\rm EFF-\Delta_L}} I_{D,\rm SAT} \tag{167}$$

$$I_{D,\rm SAT} = K_P \frac{W_{\rm EFF}}{L_{\rm EFF}} F_G F_D \left[V_{GSX} - V_T - \frac{1+F_{\rm B}}{2} V_{DS,\rm SAT} \right] V_{DS,\rm SAT} \tag{168}$$

The reduction in the channel length due to V_{DS} modulation is

$$\Delta_L = \begin{cases} \Delta'_L & \Delta'_L < \frac{1}{2} L_{\rm EFF} \\ L_{\rm EFF} - \frac{L_{\rm EFF}}{\Delta'_L} & \Delta'_L \geq \frac{1}{2} L_{\rm EFF} \end{cases} \tag{169}$$

where the punch through approximation is used for $\Delta'_L \geq \frac{1}{2} L_{\rm EFF}$¿ In (169) the distance that the depletion region at the drain extends into the channel is

$$\Delta'_L = \sqrt{\left(\frac{E_P X_D^2}{2} \right)^2 + \kappa X_D^2 (V_{DS} - V_{DS,\rm SAT})} - \frac{E_P X_D^2}{2} \tag{170}$$

and

$$E_P = \frac{I_{D,\rm SAT}}{G_{DS,\rm SAT} L_{\rm EFF}} \tag{171}$$

Here

$$G_{DS,\rm SAT} = \frac{\partial I_{D,\rm SAT}}{\partial V_{DS,\rm SAT}} \tag{172}$$

The `LEVEL` 3 current-voltage parameter dependencies are summarized in figure 10.

`LEVEL` *3 Overlap Capacitances*

In the `LEVEL 3` model the gate overlap capacitances asre strong functions of voltage. Two overlap capacitance models are available the Meyer model based on the model originally proposed by Meyer [**?**] and the Ward-Dutton model [**?**, **?**]. These models differ in the derivation of the channel charge.

`LEVEL` *3 Meyer Model*

. This model is selected when the parameter `XQC` $= X_{QC}$ is not specified or $X_{QC} < 0.5$.

The voltage dependent thin-oxide capacitances are used only if T_{OX} is specified in the model statement.

Four operating regions are defined in the Meyer model:

accumulation region:	$V_{GS} < V_{\rm ON} - 2\phi_B$
depletion region:	$V_{\rm ON} - 2\phi_B < V_{GS} < V_{\rm ON}$
saturation region:	$V_{\rm ON} < V_{GS} < V_{\rm ON} + V_{DS}$
linear region:	$V_{GS} > V_{\rm ON} + V_{DS}$

where

$$
\begin{aligned}
V_{\rm ON} &= \begin{cases} V_T + x_n V_{\rm TH} & \text{if } N_{\rm FS} = \texttt{NFS} \text{ specified} \\ V_T & \text{if } N_{\rm FS} = \texttt{NFS} \text{ not specified} \end{cases} && (173)\\
V_T &= V_{T0} + \gamma\left[\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B}\right] && (174)\\
x_n &= 1 + \frac{qN_{\rm FS}}{C'_{OX}} + \frac{C_D}{C'_{OX}} && (175)\\
C'_{OX} &= \frac{\epsilon_{OX}}{T_{OX}} && (176)\\
C_{OX} &= C'_{OX} W_{\rm EFF} L_{\rm EFF} && (177)\\
C_D &= \frac{\gamma}{2\sqrt{2\phi_B - V_{BS}}} && (178)
\end{aligned}
$$

$$
C_{GS} = \begin{cases} C_{GSO}W & \text{accumulation region} \\ \frac{2}{3}C_{OX}\left(1 + \frac{V_{\rm ON} - V_{GS}}{2\phi_B}\right) + C_{GSO}W_{\rm EFF} & \text{depletion region} \\ \frac{2}{3}C_{OX} + C_{GSO}W_{\rm EFF} & \text{saturation region} \\ C_{OX}\left\{1 - \left[\frac{V_{GS} - V_{DS} - V_{\rm ON}}{2(V_{GS} - V_{\rm ON}) - V_{DS}}\right]^2\right\} + C_{GSO}W_{\rm EFF} & \text{linear region} \end{cases} \quad (179)
$$

$$
C_{GD} = \begin{cases} C_{GDO}W_{\rm EFF} & \text{accumulation region} \\ C_{GDO}W_{\rm EFF} & \text{depletion region} \\ C_{GDO}W_{\rm EFF} & \text{saturation region} \\ C_{OX}\left\{1 - \left[\frac{V_{GS} - V_{\rm ON}}{2(V_{GS} - V_{\rm ON}) - V_{DS}}\right]^2\right\} + C_{GDO}W_{\rm EFF} & \text{linear region} \end{cases} \quad (180)
$$

$$
C_{GB} = \begin{cases} C_{OX} + C_{GBO}L_{\rm EFF} & \text{accumulation region} \\ C_{OX}\left(\frac{V_{\rm ON} - V_{GS}}{2\phi_B}\right) + C_{GBO}L_{\rm EFF} & \text{depletion region} \\ C_{GBO}L_{\rm EFF} & \text{saturation region} \\ C_{GBO}L_{\rm EFF} & \text{linear region} \end{cases} \quad (181)
$$

LEVEL *3 Ward-Dutton Model*

This model is selected when the parameter `XQC` is specified and less than 0.5. The charge in the gate Q_G and the substrate Q_B is calculated and the difference of these is taken as the channel charge $Q_{\rm CHANNEL}$. This charge is then partitioned and allocated between the source as Q_S and the drain Q_D as follows:

$$\begin{aligned} Q_{\rm CHANNEL} &= Q_D + Q_S && (182)\\ Q_D &= X_{QC} Q_{\rm CHANNEL} && (183)\\ & && (184) \end{aligned}$$

so that $Q_S = (1 - X_{QC})Q_{\rm CHANNEL}$. This partitioning is somewhat arbitrary but produces transient results that more closely match measurements than does the Meyer capacitance model. However this is at the price of poorer convergence properties and sometimes error. This is particularly so when V_{DS} is changing sign. Two operating regions are defined in the Ward-Dutton model:

off region: $V_{GS} \le V_T'$
on region: $V_{GS} > V_T'$

where

$$\begin{aligned} V_T' &= v_{BIX} + F_C && (185)\\ v_{BIX} &= V_{FB} - \sigma V_{DS} && (186) \end{aligned}$$

F_C is defined in (143), σ in (149) and V_{FB} is defined in (17) or (17). off region

$$\begin{aligned} Q_G &= \begin{cases} \gamma F_S C_{\rm OX}\left[\sqrt{\left(\frac{\gamma F_S}{2}\right)^2 + (v_{GB} - V_{FB} + 2\phi_B)} - \frac{\gamma F_S}{2}\right] & v_{GB} > (V_{FB} - 2\phi_B)\\ C_{\rm OX}(v_{GB} - V_{FB} + 2\phi_B) & v_{GB} \le (V_{FB} - 2\phi_B) \end{cases} && (187)\\ Q_B &= -Q_G && (188) \end{aligned}$$

on region

$$Q_G = \begin{cases} C_{\rm OX}(V_{GS} - V_{FB}) & V_{DSX} = 0 \\ C_{\rm OX}(V_{GS} - v_{BIX} - \frac{1}{2}V_{DSX} + x_a) & V_{DSX} \neq 0 \end{cases} \quad (189)$$

$$Q_B = \begin{cases} -C_{\rm OX}F_C & V_{DSX} = 0 \\ -C_{\rm OX}(F_C + \frac{1}{2}F_B V_{DSX} - x_a F_B) & V_{DSX} \neq 0 \end{cases} \quad (190)$$

where

$$x_a = \frac{(1+F_B)V_{DSX}^2}{12V_{GSX} - V_T' - \frac{1}{2}(1+F_B)V_{DSX}} \quad (191)$$

$$Q_{\rm CHANNEL} = -(Q_G + Q_B) \quad (192)$$

where F_B is defined in (158), V_{GSX} in (153) and

$$V_{DSX} = \begin{cases} V_{DS,\rm SAT} & V_{DS} > V_{D,\rm SAT} \\ V_{DS} & V_{DS} \leq V_{D,\rm SAT} \end{cases} \quad (193)$$

The overlap capacitances are then evaluated as

$$C_{GDB} = \partial Q_G/\partial v_D \quad (194)$$
$$C_{GSB} = \partial Q_G/\partial v_S \quad (195)$$
$$C_{GGB} = \partial Q_G/\partial v_G \quad (196)$$
$$C_{BDB} = \partial Q_B/\partial v_D \quad (197)$$
$$C_{BSB} = \partial Q_B/\partial v_S \quad (198)$$
$$C_{BGB} = \partial Q_B/\partial v_G \quad (199)$$

The overlap capacitance parameter dependencies are summarized in figure 11.

BSIM1 (LEVEL 4) MOSFET models.

The parameters of the BSIM1 (`LEVEL 4` model are all values obtained from process characterization, and can be generated automatically. J. Pierret [**?**] describes a means of generating a 'process' file, and the program Proc2Mod provided in the UC Berkeley standard SPICE3 distribution converts this file into a sequence of .MODEL lines suitable for inclusion in a SPICE circuit file. Parameters marked below with an * in the L/W column also have corresponding parameters with a length and width dependency.

Unlike most other models the BSIM1 model is designed for use with a process characterization system that provides all the parameters, thus there are no defaults for the parameters, and leaving one out is considered an error.

Table 5 continued: BSIM (`LEVEL`*) 4 model keywords.*

Name	Description	Units	Default	L/W
K2	drain/source depletion charge sharing coefficient (K_2)	-	REQUIRED	*
MJ	grading coefficient of source-drain junction (M_J)	-	REQUIRED	
MJSW	grading coefficient of source-drain junction sidewall ($M_{J,\mathrm{SW}}$)	-	REQUIRED	
MUS	mobility at zero substrate bias and at $V_{DS} = V_{DD}$ (μ_S)	$\mathrm{cm}^2/\mathrm{V}^2\mathrm{s}$	REQUIRED	*
MUZ	zero-bias mobility (μ_Z)	$\mathrm{cm}^2/\mathrm{Vs}$	REQUIRED	
N0	zero-bias subthreshold slope coefficient (N-zero) (N_0)	-	REQUIRED	*
NB	sensitivity of subthreshold slope to substrate bias (PARASITIC) (N_B)	-	REQUIRED	*
ND	sensitivity of subthreshold slope to drain bias (N_D)	-	REQUIRED	*
PB	built in potential of source/ drain junction (ϕ_J)	V	REQUIRED	
PBSW	built in potential of source/ drain juntion sidewall (PARASITIC) ($\phi_{J,\mathrm{SW}}$)	V	REQUIRED	
PHI	surface inversion potential ($2\phi_B$)	V	REQUIRED	*
RSH	drain and source diffusion sheet resistance (PARASITIC) (R_{SH})	Ω-square	REQUIRED	
TEMP	temperature at which parameters were measured (T)	C	REQUIRED	
TOX	gate oxide thickness (T_{OX})	μm	REQUIRED	
U0	zero-bias transverse-field mobility degradation coefficient (U-zero (U_0)	V^{-1}	REQUIRED	*
U1	zero-bias velocity saturation coefficient (U_1)	μm/V	REQUIRED	*
VDD	measurement bias range (V_{DD})	V	REQUIRED	
WDF	source-drain junction default width (W_{DF})	m	REQUIRED	
VFB	flat-band voltage (V_{FB})	V	REQUIRED	*
X2E	sensitivity of drain-induced barrier lowering effect to substrate bias (X_{2E})	V^{-1}	REQUIRED	*
X2MS	sensitivity of mobility to substrate bias at $V_{DS} = V_{DD}$ ($X_{2\mathrm{MS}}$)	$\mathrm{cm}^2/\mathrm{V}^2\mathrm{s}$	REQUIRED	*

Table 5 continued: BSIM (LEVEL) 4 model keywords.

Name	Description	Units	Default	L/W
X2MZ	sensitivity of mobility to substrate bias at $V_{DS} = 0$ (X_{2MZ})	cm^2/V^2s	REQUIRED	*
X2U0	sensitivity of transverse field mobility degradation effect to substrate bias (X2U-zero) (X_{2U0})	V^{-2}	REQUIRED	*
X2U1	sensitivity of velocity saturation effect to substrate bias (X_{2U1})	μmV^{-2}	REQUIRED	*
X3E	sensitivity of drain-induced barrier lowering effect to drain bias at $V_{DS} = V_{DD}$ (X_{3E})	V^{-1}	REQUIRED	*
X3MS	sensitivity of mobility to drain bias at $V_{DS}= V_{DD}$ (X_{3MS})	cm^2/V^2s	REQUIRED	*
X3U1	sensitivity of velocity saturation effect on drain bias at $V_{DS} = V_{DD}$ (X_{3U1})	μV^{-2}	REQUIRED	*
XPART	gate oxide capacitance charge partition model flag (X_{PART}) XPART = 0: selects a 40:60 drain:source charge partition XPART = 1: selects a 0:100 drain:source charge partition	-	REQUIRED	

Table 6 continued: BSIM (LEVEL) 4 model keywords, PSPICE*extensions.*

Name	Description	Units	Default
JSSW	bulk junction sidewall current per unit length (PARASITIC) $(J_{S,SW})$	A/m	0
RB	bulk ohmic resistance (PARASITIC) (R_B)	Ω	0
RD	drain ohmic resistance (PARASITIC) (R_D)	Ω	0
RDS	drain-source shunt resistance (R_{DS})	Ω	0
RG	gate ohmic resistance (PARASITIC) (R_B)	Ω	0
RS	source ohmic resistance (PARASITIC) (R_S)	Ω	0
TT	bulk p-n transit time (τ_T)	s	0
W	channel width (W)	m	DEFL

AC Analysis

. The AC analysis uses the model of figure 1 with the capacitor values evaluated at the DC operating point with

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{200}$$

and

$$R_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}} \tag{201}$$

Noise Analysis

. The MOSFET noise model accounts for thermal noise generated in the parasitic resistances and shot and flicker noise generated in the drain source current generator. The rms (root-mean-square) values of thermal noise current generators shunting the four parasitic resistance R_B, R_D, R_G and R_S are

$$I_{n,B} = \sqrt{4kT/R_B}\ \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{202}$$

$$I_{n,D} = \sqrt{4kT/R_D}\ \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{203}$$

$$I_{n,G} = \sqrt{4kT/R_G}\ \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{204}$$

$$I_{n,S} = \sqrt{4kT/R_S}\ \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{205}$$

The rms value of noise current generators in series with the drain-source current generator

$$I_{n,DS} = \left(I^2_{\mathrm{SHOT},DS} + I^2_{\mathrm{FLICKER},DS}\right)^{1/2} \tag{206}$$

$$I_{\mathrm{SHOT},DS} = \sqrt{4kTg_m\frac{2}{3}}\quad \mathrm{A}/\sqrt{\mathrm{Hz}}\ \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{207}$$

$$I_{\mathrm{FLICKER},DS} = \sqrt{\frac{K_F I_D^{A_F}}{fK_{\mathrm{CHANNEL}}}}\quad \mathrm{A}/\sqrt{\mathrm{Hz}} \tag{208}$$

where the transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{209}$$

is evaluated at the DC operating point, and

$$K_{\mathrm{CHANNEL}} = \frac{\partial L^2_{\mathrm{EFF}}\epsilon_{\mathrm{Si}}}{\partial T_{OX}} \tag{210}$$

Notes:
The actual element in *f*REEDA™is the M element. See M for full documentation.

Credits:

Name	Affiliation	Date	Links
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Table 2: MOSFET model keywords for LEVELs 1, 2, 3 continued.

Name	Description	Units	Default
FC	coefficient for forward-bias depletion capacitance formula (PARASITIC) (F_C)	-	0.5
GAMMA	bulk threshold parameter (γ)	$V^{\frac{1}{2}}$	INFERRED
IS	bulk junction saturation current (PARASITIC) (I_S)	A	10^{-14}
JS	bulk junction saturation current per sq-meter of junction area (PARASITIC) (J_S)	A/m^2	0
KAPPA	saturation field factor (LEVEL=3 only) (κ)	-	0.2
KF	flicker noise coefficient (K_F)	-	0
KP	transconductance parameter (K_P)	A/V^2	2.10^{-5}
LAMBDA	channel-length modulation (LEVEL=1, 2 only) (λ)	$1/V$	0
LD	lateral diffusion (X_{JL})	m	0
LEVEL	model index	-	1
MJ	bulk junction bottom grading coefficient (PARASITIC) (M_J)	-	0.5
MJSW	bulk junction sidewall grading coefficient (PARASITIC) ($M_{J,\mathrm{SW}}$)	-	0.33
NSUB	substrate doping (N_B)	cm^{-3}	INFERRED
NSS	surface state density (N_{SS})	cm^{-2}	INFERRED
NFS	fast surface state density (N_{FS})	cm^{-2}	0
NEFF	total channel charge (fixed and mobile) coefficient (LEVEL=2 only) (N_{EFF})	-	1
PB	bulk junction potential (ϕ_J) (This is the interface potential in the channel relative to the source at threshold.)	V	0.8
PHI	surface inversion potential ($2\phi_B$)	V	0.6
RD	drain ohmic resistance (PARASITIC) (R_D)	Ω	0
RS	source ohmic resistance (PARASITIC) (R_S)	Ω	0
RSH	drain and source diffusion sheet resistance (PARASITIC) (R_{SH})	Ω/square	0
THETA	mobility modulation (LEVEL=3 only) (θ)	$1/V$	0
TOX	oxide thickness (T_{OX}) Default for LEVEL 2 and 3 is 0.1 μm. If LEVEL 1 and TOX is omitted then the process oriented model is not used.	m	-

Table 3: MOSFET model keywords for LEVELs 1, 2, 3 continued.

Name	Description	Units	Default
TPG	type of gate material: (T_{PG}) 1 → polysilicon, opposite type to substrate −1 → polysilicon, same type as substrate 0 → aluminum gate	-	1
UCRIT	critical field for mobility degradation (LEVEL=2 only) (U_C)	V/cm	10^4
UEXP	critical field exponent in mobility degradation (LEVEL=2 only) (U_{EXP})	-	0
UO	surface mobility (U-oh) (μ_0)	cm^2/V-s	600
UTRA	transverse field coefficient (mobility) (LEVEL = 1 and 3 only) (U_{TRA})	-	0
VMAX	maximum drift velocity of carriers (V_{MAX})	m/s	0
VTO	zero-bias threshold voltage N-channel devices: positive for enhancement mode and negative for depletion mode devices. P-channel devices: negative for enhancement mode and positive for depletion mode devices. (VT-oh) (V_{T0})	V	0
XJ	metallurgical junction depth (X_J)	m	0

PROCESS PARAMETERS	
DELTA	δ
LAMBDA	λ
NSS	N_{SS}
NSUB	N_B
PB	ϕ_J
TOX	T_{OX}
UCRIT	U_C
UEXP	U_{EXP}
VMAX	V_{MAX}
UO	μ_0
XJ	X_J

+

GEOMETRY PARAMETERS	
Required	
L	L
W	W
Optional	
LD	X_{JL}
WD	W_D

→

DEVICE PARAMETERS	
I/V	
VTO	$V_{T0} = f(2\phi_B, N_{\mathrm{SS}}, T_{OX})$
KP	$K_P = f(\mu_0, T_{OX})$
PHI	$2\phi_B = f(N_B)$
GAMMA	$\gamma = f(\mu_0, T_{OX}, N_B)$
	$\{I_D = f(W, L, W_D, X_{JL},$
	$K_P, 2\phi_B, \mu_0, \gamma, V_{T0}, \phi_J$
	$V_{\mathrm{MAX}}, X_J, \lambda, U_{\mathrm{EXP}}, U_C, \delta)\}$

Figure 8: MOSFET LEVEL 2 I/V parameter relationships.

Table 4: MOSFET model keywords for LEVELs 1, 2, 3; PSPICEextensions.

Name	Description	Units	Default
JSSW	bulk p-n junction sidewall current per unit length (PARASITIC) $(J_{S,\mathrm{SW}})$	A/m	0
L	channel length (L)	m	DEFL
N	bulk p-n emission coefficient (PARASITIC) (N)	-	0
PBSW	bulk p-n sidewall potential (PARASITIC) $(\phi_{J,\mathrm{SW}})$	V	PB
RB	bulk ohmic resistance (PARASITIC) (R_B)	Ω	0
RG	gate ohmic resistance (PARASITIC) (R_B)	Ω	0
RDS	drain-source shunt resistance (R_{DS})	Ω	∞
T_ABS	(T_{ABS})	°C	current temp.
T_MEASURED	(T_{MEASURED})	°C	TNOM
T_REL_GLOBAL	$(T_{\mathrm{REL\_GLOBAL}})$	°C	0
T_REL_LOCAL	$(T_{\mathrm{REL\_LOCAL}})$	°C	0
TT	bulk p-n transit time (τ_T)	s	0
W	channel width (W)	m	DEFW
WD	lateral diffusion width (W_D)	m	0
XQC	fraction of channel charge attributable to drain in saturation region (X_{QC}) If $X_{QC} > 0.5$ the Meyer Capacitance Model is used. If $X_{QC} \leq 0.5$ the Ward-Dutton Capacitance Model is used.	-	1

PROCESS PARAMETERS	
CJ	C_J
CJSW	$C_{J,\mathrm{SW}}$
MJ	M_J
MJSW	$M_{J,\mathrm{SW}}$
PB	ϕ_J
PBSW	ϕ_J
FC	ϕ_J

+

GEOMETRY PARAMETERS	
AD	A_D
AS	A_S
PD	A_D
PS	A_S

→

DEVICE PARAMETERS	
Constant Overlap Capacitances	
CGSO	C_{GSO}
CGDO	C_{GDO}
CGBO	C_{GBO}

Figure 9: MOSFET LEVEL 2 overlap capacitance parameter relationships.

PROCESS PARAMETERS	
KAPPA	κ
NSS	N_{SS}
NSUB	N_B
PB	ϕ_J
THETA	θ
TOX	T_{OX}
UO	μ_0
VMAX	V_{MAX}
XJ	X_J

+

GEOMETRY PARAMETERS	
Required	
L	L
W	W
Optional	
LD	X_{JL}
WD	W_D

→

DEVICE PARAMETERS	
I/V	
VTO	$V_{T0} = f(2\phi_B, N_{\mathrm{SS}}, T_{OX})$
KP	$K_P = f(\mu_0, T_{OX})$
PHI	$2\phi_B = f(N_B)$
GAMMA	$\gamma = f(\mu_0, T_{OX}, N_B)$
$\{I_D = f(W, L, W_D, X_{JL}$	$K_P, 2\phi_B, N_B, T_{OX}, \mu_0, \theta$
$\gamma, V_{T0}, \phi_J, V_{\mathrm{MAX}}, X_J, \kappa, \eta)\}$	

Figure 10: MOSFET LEVEL 3 I/V parameter relationships.

PROCESS PARAMETERS	
NSUB	N_B
CJ	C_J
CJSW	$C_{J,\mathrm{SW}}$
MJ	M_J
MJSW	$M_{J,\mathrm{SW}}$
PB	ϕ_J
PBSW	$\phi_{J,\mathrm{SW}}$
FC	F_C

+

GEOMETRY PARAMETERS	
AD	A_D
AS	A_S
PD	P_D
PS	P_S

→

DEVICE PARAMETERS	
Constant Overlap Capacitances	
CGSO	C_{GSO}
CGDO	C_{GDO}
CGBO	C_{GBO}

Figure 11: MOSFET LEVEL 3 overlap capacitance parameter relationships.

Table 5: SPICE BSIM1 (level 4) parameters.

Name	Description	Units	Default	L/W
CGBO	gate-bulk overlap capacitance per meter channel length (PARASITIC) (C_{GBO})	F/m	REQUIRED	
CGDO	gate-drain overlap capacitance per meter channel width (PARASITIC) (C_{GDO})	F/m	REQUIRED	
CGSO	gate-source overlap capacitance per meter channel width (PARASITIC) (C_{GSO})	F/m	REQUIRED	
CJ	source-drain junction capacitance per unit area (PARASITIC) (C_J)	F/m^2	REQUIRED	
CJSW	source-drain junction sidewall capacitance per unit length (PARASITIC) ($C_{J,SW}$)	F/m	REQUIRED	
DL	shortening of channel (Δ_L)	μm	REQUIRED	
DW	narrowing of channel (Δ_W)	μm	REQUIRED	
DELL	source-drain junction length reduction ($DELL$)	m	REQUIRED	
ETA	zero-bias drain-induced barrier lowering coefficient (η)	-	REQUIRED	*
JS	source-drain junction current density (J_S)	A/m^2	REQUIRED	
K1	body effect coefficient (K_1)	$V^{\frac{1}{2}}$	REQUIRED	*

Table 6: SPICE BSIM1 (level 4) parameters, PSPICEextensions.

Name	Description	Units	Default
AF	flicker noise exponent (A_F)	-	1
CBD	zero-bias B-D junction capacitance (C'_{BD})	F	0
CBS	zero-bias B-S junction capacitance (C'_{BS})	F	0
FC	coefficient for forward-bias depletion capacitance formula (F_C)	-	0.5
IS	bulk junction saturation current (I_S)	A	1E-14
KF	flicker noise coefficient (K_F)	-	0
L	channel length (L)	m	DEFL
N	bulk p-n emission coefficient (PARASITIC) (N)	-	0
PBSW	bulk p-n sidewall potential (PARASITIC) ($\phi_{J,\mathrm{SW}}$)	V	PB