0.0.1 Digital Input Interface N

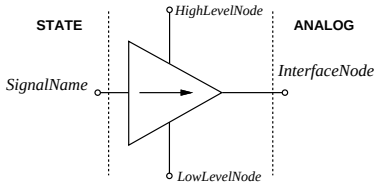

Figure 1: N — Digital input interface element. Converts from a digital (state) signal to an analog signal.

`SPICE` *Form:*
`N`name *InterfaceNode LowLevelNode HighLevelNode ModelName* [`SIGNAME =` *DigitalSignalName*] [`IS =` *InitialState*]

InterfaceNode
Identifier of node interfacing between digital signal and continuous time circuit.

LowLevelNode
Identifier of low level reference node. Normally this is the logic "zero" voltage.

HighLevelNode
Identifier of high level reference node. Normally this is the logic "one" voltage.

ModelName
Name of the model specifying transitions times and resistances and capacitances of each logic state.

`SIGNAME`
Keyword for digital signal name. (optional)

DigitalSignalName
Digital signal name.
DigitalSignalName is the name of the signal specified in the input file specified in the element model. If it is omitted then *DigitalSignalName* defaults element name `N`*name* stripped of the prefix `N` (i.e. *name*).

`IS`
Keyword for initial state. (optional)

InitialState
Integer specifying the initial state. If specified, it must be 0, 1, ..., or 19. This over rides the state specified at `TIME`=0 in the digital input file (see the model specification).
The state of the digital interface input (`N`) element remains as the *InitialState* state until a state (other than the state at `TIME`=0 is input from the specified file.

Example:

```
N100 1 0 2 INTERFACE_FROM_REGISTER SIGNAME=REG1 IS=0
NCONTROL 1 0 2 CONTROL
```

Description:
Model Type

DINPUT

The digital input interface is modeled by time variable resistances between the *Interface Node* and the *Low Level Node* and between the the *Interface Node* and the *High Level Node*. The variable resistances are shunted by fixed capacitances. The resistance are controlled by parameters specified in the model *ModelName*. The resistance varies exponentially from the old state to the new state over the time period indicated for the new state. This approximates the output of a digital gate.

N

DINPUT Model — Digital Input Interface Model

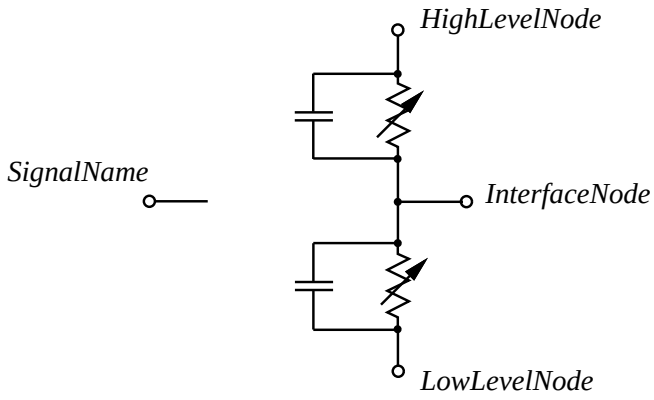

Figure 2: Digital input interface model.

Keywords:

Name	Description	Units	Default
FILE	digital input filename. If more than one model refers to the same file then the filenames specified must be identical and not logically equivalent. This ensures that the file is opened only once.	-	REQUIRED
FORMAT	digital input file format	-	1
TIMESTEP	digital input file time step	s	1NS
CLO	capacitance to low level node	F	0
CHI	capacitance to high level node	F	0
SnNAME	state "n" character abreviation n = 0, 2, ..., or 19	-	REQUIRED
SnTSW	state "n" switching time n = 0, 2, ..., or 19	s	REQUIRED
SnRLO	state "n" resistance to low level node n = 0, 2, ..., or 19	Ω	REQUIRED
SnRHI	state "n" resistance to high level node n = 0, 2, ..., or 19	Ω	REQUIRED

The digital input interface is modeled by time variable resistances between the *Interface Node* and the *Low Level Node* and between the the *Interface Node* and the *High Level Node*. The variable resistances are shunted by fixed capacitances. The parameters are controlled by parameters specified in the model. Upon a state transition the two resistances vary exponentially from the old state to the new state over the time period indicated for the new state. This approximates the output of a digital gate. The sequence of states and the state change times are specified in the file specified by the FILE = (*InputFileName*) keyword in the model. The initial state at TIME 0 is taken from this file unless the IS keyword is specified on the element line. In the I_S (= *InitialState*) keyword is specified then the state of the digital input interface is *InitialState* until a state transition at TIME > 0 is specified in the file *InputFileName*.

Notes:
There is no equivalent element in *f*REEDA™.

Credits:

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