0.0.1 Digital Output Interface O

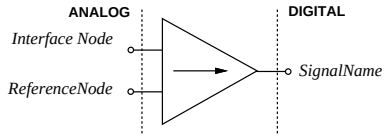

Figure 1: O — Digital output interface element.

`SPICE` *Form:*
`O`name *InterfaceNode ReferenceNode ModelName* [`SIGNAME =` *DigitalSignalName*]

InterfaceNode
: Identifier of node interfacing between digital signal and continuous time circuit.

ReferenceNode
: Identifier of reference node. Normally this is ground.

ModelName
: Name of the model specifying transitions times and resistances and capacitances of each logic state.

`SIGNAME`
: Keyword for digital signal name. (optional)

DigitalSignalName
: Digital signal name.

Example:

```
O100 1 0 INTERFACE_TO_MEMORY SIGNAME=MEM1
OADD1 1 0 2 ADD1
```

Description:
Model Type

`DOUTPUT`

The digital output interface is modeled by time variable resistances between the *Interface Node* and the *Low Level Node* and between the the *Interface Node* and the *High Level Node*. The variable resistances are shunted by fixed capacitances. The parameters are controlled by parameters specified in the model. The resistance varies exponentially from the old state to the new state over the time period indicated for the new state. This approximates the output of a digital gate.

DOUTPUT Model Digital Output Interface Model

Keywords:

Name	Description	Units	Default
FILE	digital output filename. If more than one model refers to the same file then the filenames specified must be identical and not logicly equivalent. This ensures that the file is opened only once.	-	REQUIRED
FORMAT	digital output file format	-	1
TIMESTEP	digital output file time step	s	1NS
TIMESCALE	digital output file time scale	s	1
CHGONLY	Output type flag: $= 0 \rightarrow$ output at each TIMESTEP $= 1 \rightarrow$ output only on state change	-	0
CLOAD	capacitance	F	0
RLOAD	resistance	Ω	1000
SnNAME	state "n" character abreviation n = 0, 2, ..., or 19	-	REQUIRED
SnVLO	state "n" low level voltage n = 0, 2, ..., or 19	s	REQUIRED
SnVHI	state "n" high level voltage n = 0, 2, ..., or 19	s	REQUIRED

The digital output interface is modeled by a resistance *RLoad* and capacitance *CLoad* between the *InterfaceNode* and the *Reference Node* . The values of *Rload* and *CLoad* are specified in the model *ModelName*.

A state transition from state n (n = one of 0, 1, 2, ... 19) is indicated if the interface voltage $V_{InterfaceNode} - V_{ReferenceNode}$ between the *InterfaceNode* and the *ReferenceNode* node is outside the range SnVHI − SnVLO. If there is a state transistion then the valid voltage range of each state k is considered in order from state k = 0 to state 19 to determine which voltage range SkVHI − SkVLO brackets the current interface voltage $V_{InterfaceNode} - V_{ReferenceNode}$. The first valid state becomes the new state. If there is no valid state then the new state is indeterminate and designated by "?". At each TIME being a multiple integer of TIMESTEP a line is written to the digital output file *OutputFileName*. If the new state at the time $t_i = i \cdot$ TIMESTEP is n then the i th line is:

int($i \cdot$ TIMESCALE) n

where int() is the integer operation. An example of the first few lines of *OutputFileName* with a `TIMESTEP` of 1 ns and `TIMESCALE` of 2 is:

```
0.0 1
2 0
4 2
6 3
8 ?
10 1
12 0
14 1
```

Notes:
There is no equivalent element in *f*REEDA™.

Credits:

Name	Affiliation	Date	Links
Carlos E. Christofferson	NC State University	Sept 2000	NC STATE UNIVERSITY
cechrist@ieee.org			www.ncsu.edu