

Figure 1: JFET Types (a) N-channel FET (b) P-channel FET

Form: jfetp:<instance name> n_1 n_2 n_3 <parameter list>

n_1 is the drain node,
 n_2 is the gate node,
 n_3 is the source node,

Parameters:

Parameter	Type	Default value	Required?
af: Flicker noise exponent	DOUBLE	1	no
area: Device area (m^2)	DOUBLE	1	no
beta: Transconductance parameter (A/V^2)	DOUBLE	0.0001	no
cgs: Zero bias gate source junction capacitance (F)	DOUBLE	0	no
cgd: Zero bias gate drain junction capacitance (F)	DOUBLE	0	no
eg: Barrier height at 0 K (eV)	DOUBLE	0.8	no
fc: Coefficient for forward bias depletion capacitance	DOUBLE	0.5	no
is: Gate junction saturation current (A)	DOUBLE	1×10^{-14}	no
kf: Flicker noise coefficient	DOUBLE	0	no
pb: Gate junction potential (1/V)	DOUBLE	0	no
rd: Drain ohmic resistance (ω)	DOUBLE	0	no
rs: Source ohmic resistance (ω)	DOUBLE	0	no
vt0: Threshold voltage (V)	DOUBLE	-2	no
m: Gate p-n grading coefficient	DOUBLE	0.5	no
vt0tc: Temperature coefficient for vt0 (V/K)	DOUBLE	0.0	no
tnom: Nominal temperature (K)	DOUBLE	300	no
b: Doping tail parameter	DOUBLE	1	no
t: Device temperature (K)	DOUBLE	300	no
lambda: Channel length modulation parameter (1/V)	DOUBLE	0	no

Example:

jfetp:j1 3 4 2 beta=0.0001

Description:

fREEDATM has the PJFET model based on the PJF model in SPICE.

DC Calculations:

Constants used are:

$$q = 1.6021918 \times 10^{-19} (As) \quad (1)$$

$$k = 1.3806226 \times 10^{-23} (J/K) \quad (2)$$

All parameters used are indicated in **this** font. The equations for the P-channel FET are identical to the N-channel except that the signs on the voltages and the output are reversed.

The current/voltage characteristics are evaluated after first determining the mode (normal: $V_{SD} \geq 0$ or inverted: $V_{SD} < 0$) and the region (cutoff, linear or saturation) of the current (V_{SD}, V_{SG}) operating point.

Normal Mode: ($V_{SD} \geq 0$)

Regions of operation:

$$\begin{array}{ll} V_{SG} - V_{T0} \leq 0 & \text{Cutoff Region} \\ 0 \leq V_{SD} < V_{SG} - V_{T0} & \text{Linear Region} \\ 0 < V_{SG} - V_{T0} \leq V_{SD} & \text{Saturation Region} \end{array}$$

Then

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ \text{AREA} \times \text{BETA} (1 + \text{LAMBDA} V_{SD}) V_{SD} [2 (V_{SG} - V_{T0}) - V_{SD}] & \text{linear region} \\ \text{AREA} \times \text{BETA} (1 + \text{LAMBDA} V_{SD}) (V_{SG} - V_{T0})^2 & \text{saturation region} \end{cases} \quad (3)$$

Inverted Mode: ($V_{SD} < 0$)

Regions of operation:

$$\begin{array}{ll} V_{DG} - V_{T0} \leq 0 & \text{Cutoff Region} \\ 0 \leq -V_{SD} < V_{DG} - V_{T0} & \text{Linear Region} \\ 0 < V_{DG} - V_{T0} \leq -V_{SD} & \text{Saturation Region} \end{array}$$

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ \text{AREA} \times \text{BETA} (1 - \text{LAMBDA} V_{SD}) V_{SD} [2 (V_{DG} - V_{T0}) + V_{SD}] & \text{linear region} \\ \text{AREA} \times (-\text{BETA}) (1 - \text{LAMBDA} V_{SD}) (V_{DG} - V_{T0})^2 & \text{saturation region} \end{cases} \quad (4)$$

Leakage Currents

Current flows across the normally reverse biased source-bulk and drain-bulk junctions. The gate-source leakage current

$$I_{GS} = \text{AREA} \times I_S e^{(V_{SG}/V_{T0} - 1)} \quad (5)$$

and the gate-source leakage current

$$I_{GD} = \text{AREA} \times I_S e^{(V_{DG}/V_{T0} - 1)} \quad (6)$$

Capacitances

The drain-source capacitance

$$C_{DS} = \text{AREA} \times \text{CDS} \quad (7)$$

The gate-source capacitance

$$C_{GS} = \begin{cases} \text{AREA} \times \text{CGS} \left(1 - \frac{V_{SG}}{\text{PB}}\right)^{-M} & V_{SG} \leq \text{FC} \times \text{PB} \\ \text{AREA} \times \text{CGS} (1 - \text{FC})^{-(1+M)} \left[1 - \text{FC}(1 + M) + M \frac{V_{SG}}{\text{PB}}\right]^{-M} & V_{SG} > \text{FC} \times \text{PB} \end{cases} \quad (8)$$

models charge storage at the gate-source depletion layer. The gate-drain capacitance

$$C_{GD} = \begin{cases} \text{AREA} \times \text{CGD} \left(1 - \frac{V_{DG}}{\text{PB}}\right)^{-\text{M}} & V_{DG} \leq \text{FC} \times \text{PB} \\ \text{AREA} \times \text{CGD} (1 - \text{FC})^{-(1+\text{M})} \left[1 - \text{FC}(1 + \text{M}) + \text{M} \frac{V_{DG}}{\text{PB}}\right]^{-\text{M}} & V_{DG} > \text{FC} \times \text{PB} \end{cases} \quad (9)$$

models charge storage at the gate-drain depletion layer.


Notes:

This is the J element in the SPICE compatible netlist.

Version:

2001.05.15

Credits:

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