Junction Field Effect Transistor J

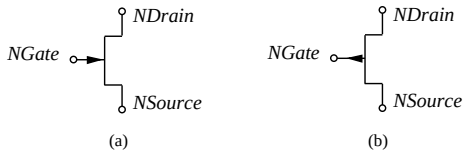

Figure 1: J — JFET element (a) n-channel JFET ; (b) p-channel JFET

`SPICE` *Form*:
`J`name NDrain NGate NSource ModelName [Area] [`OFF`] [`IC=`Vbe,Vce]

NDrain	is the drain node.
NGate	is the gate node.
NSource	is the source node.
ModelName	is the model name.
Area	is the area factor.(Units: none; Optional; Default: 1; Symbol: *Area*)
`OFF`	indicates an (optional) initial condition on the device for the dc analysis. If specified the dc operating point is calculated with the terminal voltages set to zero. Once convergence is obtained, the program continues to iterate to obtain the exact value of the terminal voltages. The OFF option is used to enforce the solution to correspond to a desired state if the circuit has more than one stable state.
`IC`	is the optional initial condition specification using `IC=`V_{BE}, V_{CE} is intended for use with the `UIC` option on the `.TRAN` line, when a transient analysis is desired starting from other than the quiescent operating point. See the *.IC* line description for a better way to set transient initial conditions.

Example:
J2 12 10 3 OFF
Model Parameters:

The parameters remain the same for an n-channel and p-channel JFET

Name	Description	Units	Default
AF	flicker noise exponent (A_F)	-	1
BETA	transconductance parameter (β)	A/V^2	1.0E-4
CGS	zero-bias G-S junction capacitance per unit area (C'_{GS})	F	0
CGD	zero-bias G-D junction capacitance per unit area (C'_{GD})	F	0
FC	coefficient for forward-bias depletion capacitance formula (F_C)	-	0.5
IS	gate junction saturation current (I_S)	A	1.0E-14
KF	flicker noise coefficient (K_F)	-	0
LAMBDA	channel length modulation parameter (λ)	1/V	0
PB	gate junction potential (ϕ_J)	V	1
RD	drain ohmic sheet resistance (R_D)	Ω	0
RS	source ohmic sheet resistance (R_S)	Ω	0
VTO	threshold voltage (V_{T0}) VTO < 0 indicates a depletion mode JFET VTO ≥ 0 indicates an enhancement mode JFET	V	-2.0
BETATC	temperature coefficient of BETA ($T_{C,\beta}$)	/°C	0
M	gate p-n junction grading coefficient (M)	-	0.5
VTOTC	temperature coefficient of threshold voltage VTO ($T_{C,VT0}$)	V/°C	0

Description:
JFET Model:

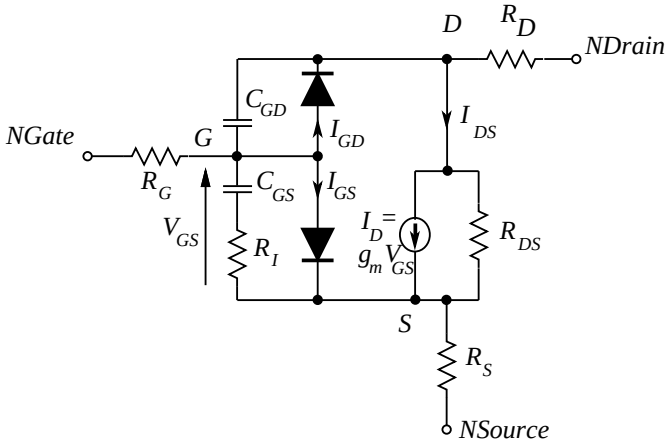

Figure 2: Schematic of the JFET Model

The physical constants used in the model evaluation are

k	Boltzmann's constant	$1.3806226\,10^{-23}$ J/K
q	electronic charge	$1.6021918\,10^{-19}$ C

Standard Calculations:

Absolute temperatures (in kelvins, K) are used. The thermal voltage

$$V_{TH} = \frac{kT_{NOM}}{q}. \tag{1}$$

The silicon bandgap energy

$$E_G = 1.16 - 0.000702\frac{4T_{NOM}^2}{T_{NOM} + 1108}. \tag{2}$$

Current Characteristics:

The current/voltage characteristics are evaluated after first determining the mode (normal: $V_{DS} \geq 0$ or inverted: $V_{DS} < 0$) and the region (cutoff, linear or saturation) of the current (V_{DS}, V_{GS}) operating point.

Normal Mode: ($V_{DS} \geq 0$)

Regions of operation:

$V_{GS} - V_{T0} \leq 0$	Cutoff Region
$0 \leq V_{DS} < V_{GS} - V_{T0}$	Linear Region
$0 < V_{GS} - V_{T0} \leq V_{DS}$	Saturation Region

Then

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ Area\,\beta\,(1 + \lambda V_{DS})\,V_{DS}\,[2\,(V_{GS} - V_{T0}) - V_{DS}] & \text{linear region} \\ Area\,\beta\,(1 + \lambda V_{DS})\,(V_{GS} - V_{T0})^2 & \text{saturation region} \end{cases} \tag{3}$$

Inverted Mode: ($V_{DS} < 0$)

Regions of operation:

$V_{GD} - V_{T0} \leq 0$	Cutoff Region
$0 \leq -V_{DS} < V_{GD} - V_{T0}$	Linear Region
$0 < V_{GD} - V_{T0} \leq -V_{DS}$	Saturation Region

$$I_D = \begin{cases} 0 & \text{cutoff region} \\ Area\,\beta\,(1 - \lambda V_{DS})\,V_{DS}\,[2\,(V_{GD} - V_{T0}) + V_{DS}] & \text{linear region} \\ Area\,(-\beta)\,(1 - \lambda V_{DS})\,(V_{GD} - V_{T0})^2 & \text{saturation region} \end{cases} \tag{4}$$

Leakage Currents:

Current flows across the normally reverse biased source-bulk and drain-bulk junctions. The

gate-source leakage current

$$I_{GS} = Area\, I_S e^{(V_{GS}/V_{TH} - 1)} \tag{5}$$

and the gate-source leakage current

$$I_{GD} = Area\, I_S e^{(V_{GD}/V_{TH} - 1)} \tag{6}$$

Capacitances:

The drain-source capacitance

$$C_{DS} = Area\, C'_{DS} \tag{7}$$

The gate-source capacitance

$$C_{GS} = \begin{cases} Area\, C'_{GS} \left(1 - \frac{V_{GS}}{\phi_J}\right)^{-M} & V_{GS} \leq F_C \phi_J \\ Area\, C'_{GS} \left(1 - F_C\right)^{-(1+M)} \left[1 - F_C(1+M) + M\frac{V_{GS}}{\phi_J}\right]^{-M} & V_{GS} > F_C \phi_J \end{cases} \tag{8}$$

models charge storage at the gate-source depletion layer. The gate-drain capacitance

$$C_{GD} = \begin{cases} Area\, C'_{GD} \left(1 - \frac{V_{GD}}{\phi_J}\right)^{-M} & V_{GD} \leq F_C \phi_J \\ Area\, C'_{GD} \left(1 - F_C\right)^{-(1+M)} \left[1 - F_C(1+M) + M\frac{V_{GD}}{\phi_J}\right]^{-M} & V_{GD} > F_C \phi_J \end{cases} \tag{9}$$

models charge storage at the gate-drain depletion layer.
Notes:
The actual element is the `jfet` TRANSIM element. See TRANSIM element `jfet` for full documentation.

Credits:

Name	Affiliation	Date	
Nikhil Kriplani	North Carolina State University	April 2001	NC STATE UNIVERSITY
Shubha Vijaychand	North Carolina State University	April 2001	NC STATE UNIVERSITY