ENGI 5131 --- Tutorial

ACM Parameter Extraction from Simulations

Lakehead University

Peter Luong, Carlos Christoffersen

Winter 2016, 2017

SECTION 1) PURPOSE:

1/ To allow the extraction of several MOSFET design parameters:

(A) I_{SQ}: sheet-specific current
(B) V_T: threshold voltage
(C) n: slope factor
(D) dL / dV_{DS}: channel length modulation

SECTION 2) MOTIVATION:

1/ The advanced compact MOSFET (ACM) model has several advantages in a MOSFET-only design;

2/ It is a single set of formulas that apply to any operating region of the MOSFET (weak, moderate, strong inversion), facilitating designs that can be optimized for low-power and low-area at the same time.

3/ The ACM model describes MOSFET currents and voltages as follows[1]:

DRAIN CURRENT:

EQ.2.1:

$$I_D = \frac{W}{L} I_{SQ} \left(i_F - i_R\right)$$

EQ.2.2:

$$I_{SQ} = \frac{1}{2}\, n\, \mu\, C_{OX}\, {V_{TH}}^2$$

GATE/SOURCE/DRAIN VOLTAGES:

EQ.2.3:

$$F(i_{F(R)}) = \sqrt{1 + i_{F(R)}} - 2 + \mathrm{LN}\left(\sqrt{1 + i_{F(R)}} - 1\right)$$

EQ.2.4:

$$F(i_{F(R)}) = \frac{|V_{GB}| - |V_T|}{nV_{TH}} - \frac{|V_{SB(DB)}|}{V_{TH}}$$

LEGEND (in order of appearance):	
I_D = transistor drain current	u = mobility of electrons of holes
W = transistor gate width	C_{OX} = gate oxide capacitance
L = transistor gate length	V_{TH} = thermal voltage (~25.8mV @ 300K)
I_{SQ} = the sheet-specific current	V_{GB} = gate voltage referenced to the bulk
i_F = forward inversion coefficient	V_{SB} = source voltage referenced to the bulk
i_R = reverse inversion coefficient	V_{DB} = drain voltage referenced to the bulk
n = slope factor	

4/ As can be seen from EQ.2.1 – EQ.2.4, the ACM model relies on parameters such as the slope factor and sheet-specific current, which usually are not provided by typical transistor technology datasheets.

1 NOTE: For a more complete coverage of the ACM model, the reader should refer to [1] or [2].

5/ Moreover, the threshold voltage as defined by the ACM model is different than that defined in a more traditional model [1].

6/ Hence in the absence of ACM-based information, the designer needs to extract their own parameters with the aid of certain circuit simulation techniques.

SECTION 3) DOCUMENT ORGANIZATION:

1/ The document will be organized as follows:

2/ First the extraction circuits and techniques will be presented.

3/ Then theoretical basis of such techniques will be justified.

SECTION 4) ASSUMPTIONS PRIOR TO USE:

1/ Though techniques in this document should apply universally to all technologies, it is assumed that:

(A) circuits are being simulated, as opposed to a physical chip test

(B) the Cadence simulator + a BSIM model of transistors are used

(C) preliminary initialization / usage of Cadence is known

(D) examples in the tutorial will be based on the TSMC 180 nm technology

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SECTION 5) EXTRACTION CIRCUITS

1/ The extraction circuits are as follows:

FIG.5.1: ISQ, VT

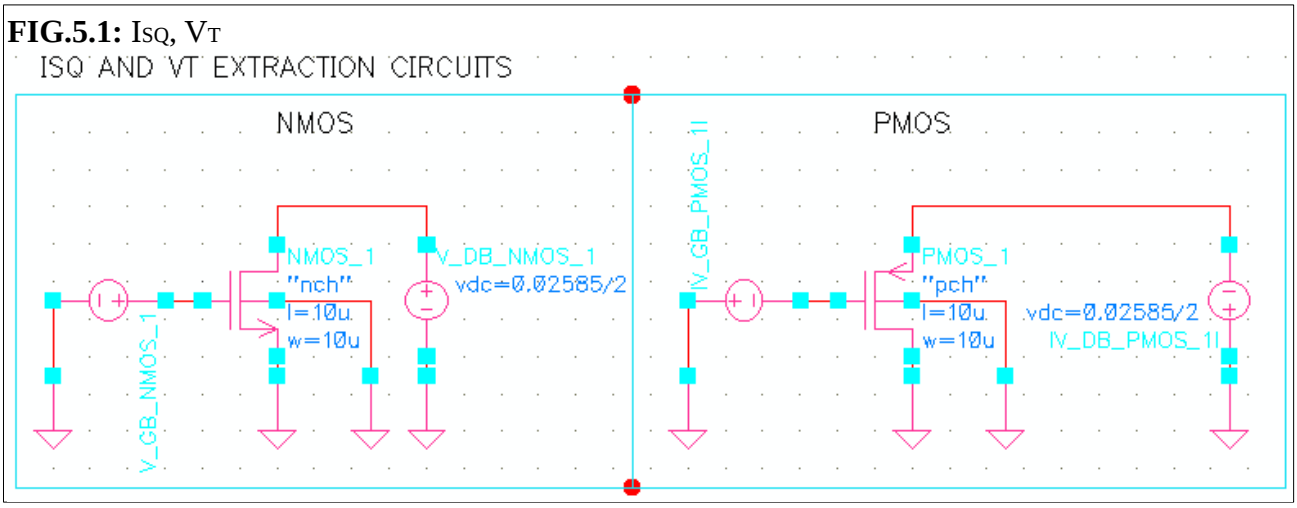


FIG.5.2: SLOPE FACTOR

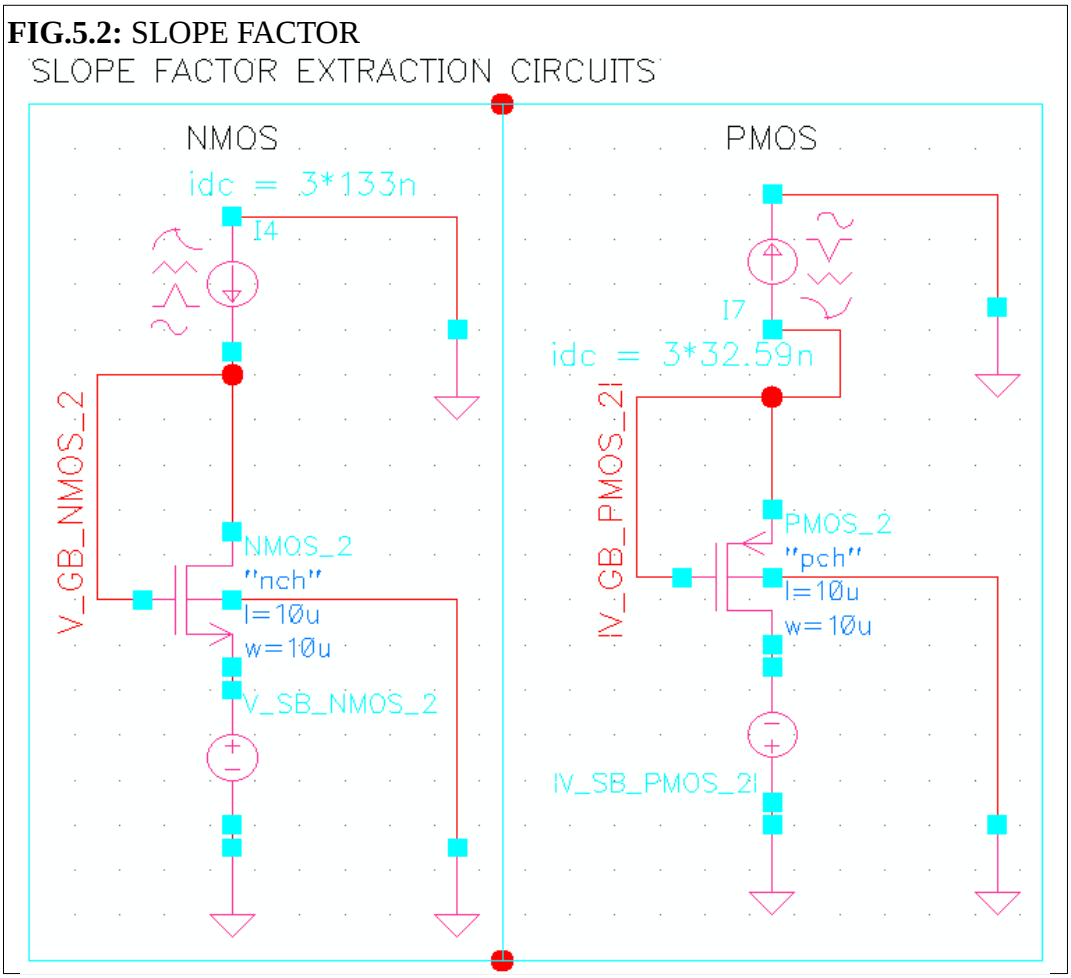
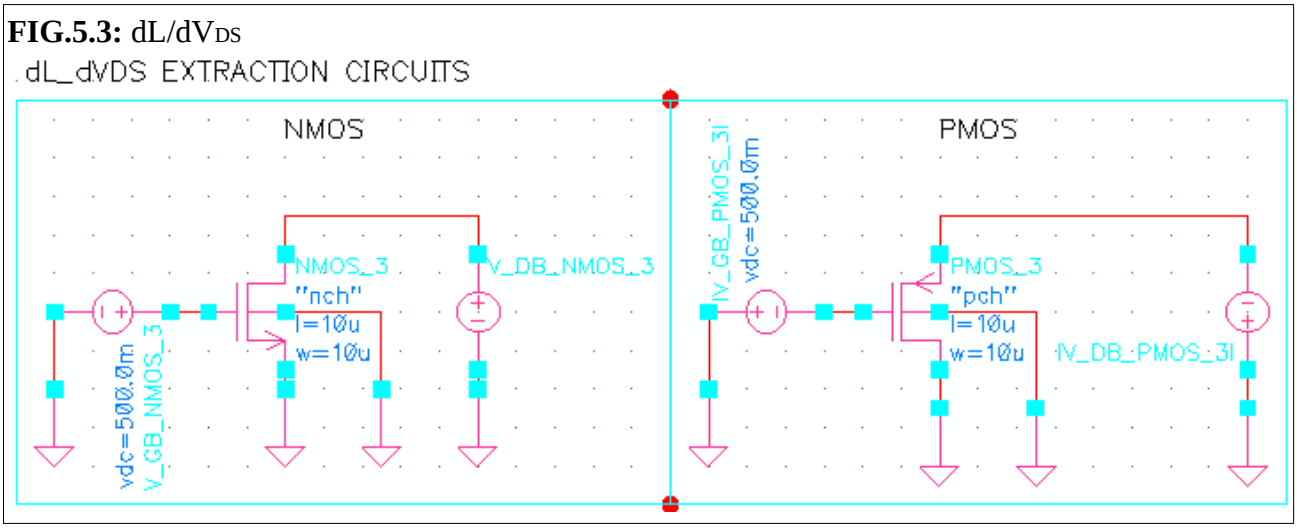


FIG.5.3: dL/dV$_{DS}$



Notes:

2/ In FIG.5.1, the |V$_{DB}$| is set at half the thermal voltage.

3/ In FIG.5.2, the DC current is set to be 3x the (W/L * I$_{SQ}$) current extracted based on the circuit from FIG.5.1.

4/ In all figures, the PMOS is identical to the NMOS circuits except all the current and voltages are reversed, due to the PMOS operating in an opposite manner to the NMOS (i.e.: a gate voltage of 0V conducts more current in a PMOS than an NMOS; a gate voltage of VDD conducts more current in an NMOS than a PMOS).

5/ In all figures, both the transistor widths and lengths are set to be large, at 10 um.
This large size is to avoid any second order effects due to small transistor dimensions.

6/ In FIG.5.2 and FIG.5.3, the names of the varying voltage sources in the PMOS circuits are technically incorrect; however doing so was found to result in more consistency and less errors during simulations.

SECTION 6) EXTRACTION CIRCUITS, COMPONENT PROPERTIES

1/ The following shows the properties of the components used throughout FIG.5.1 to FIG.5.3, with essential elements underlined

FIG.6.1: NMOS PROPERTIES

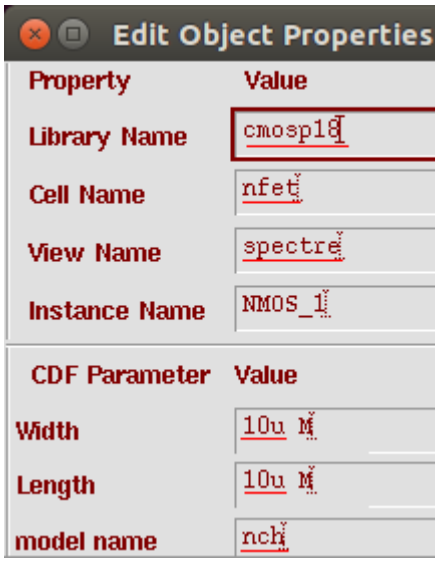


FIG.6.2: PMOS PROPERTIES

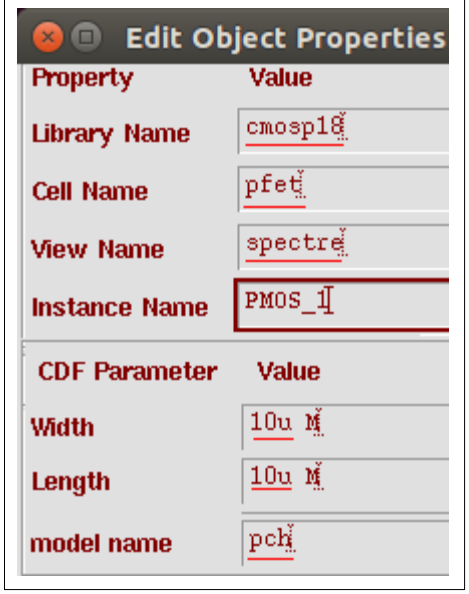


FIG.6.3: V_{DC} PROPERTIES

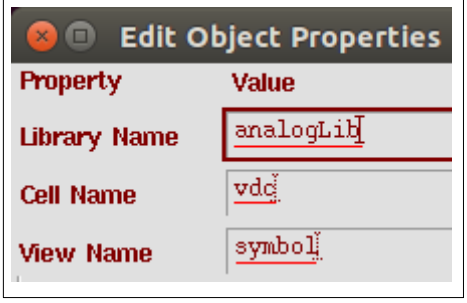
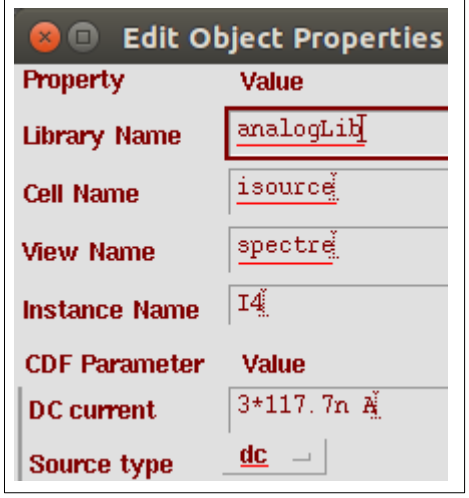


FIG.6.4: I_{DC} PROPERTIES

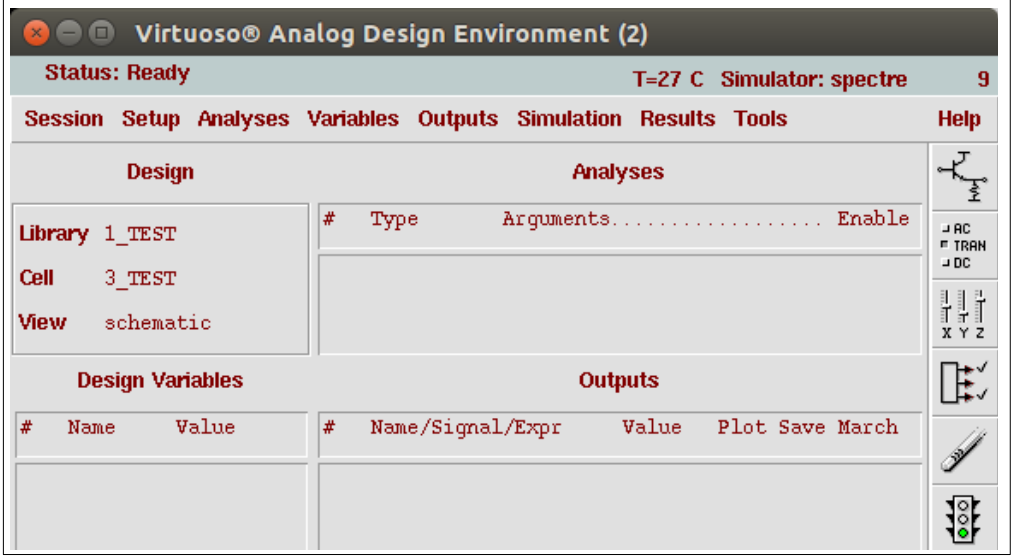


SECTION 7) SIMULATION, SETUP, INITIALIZATION

1/ To start the simulator, do the following:
Tools → Analog Environment

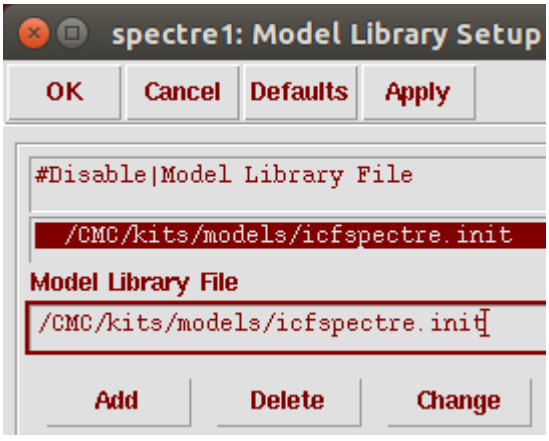
2/ The simulator should look similar to the following:

FIG.7.1: SIMULATOR



3/ To ensure the simulator will work, the model library may need to be defined; to do so, go to:
Setup → Model Libraries …

FIG. 7.2: MODEL LIBRARY



3/ Then add "**/CMC/kits/models/icfspectre.init**".

4/ The above step assumes TSMC 180 nm is used and library file is placed in that location.[2]

2 **DISCLAIMER:** Different technologies and file structures may require different files/paths specified.

SECTION 8) SIMULATION, I_{SQ}/V_T

SECTION 8.1) TECHNIQUE, I_{SQ}/V_T, BRIEF EXPLANATION:

1/ For the I_{SQ} / V_T circuits as shown in FIG.5.1, the gate voltage is varied, while analysis of the drain current + the transconductance-to-drain-current ratio (g_m/I_D) results in finding out the V_T and I_{SQ}.

2/ g_m/I_D is characterized as follows:

EQ.8.1:

$$\frac{g_m}{I_D} = \frac{\frac{dI_D}{dV_{GB}}}{I_D} = \frac{d\,\mathrm{LN}(I_D)}{d\,V_{GB}}$$

3/ The gate voltage at 53% of g_m/I_D's maximum value corresponds to the threshold voltage, V_T, as defined by the ACM model.

4/ The value of current when $|V_{GB}|= |V_T|$ divided by (0.885 * W/L) corresponds to the sheet-specific current, I_{SQ}.

SECTION 8.2) TECHNIQUE, I_{SQ}/V_T, CHOOSING ANALYSIS:

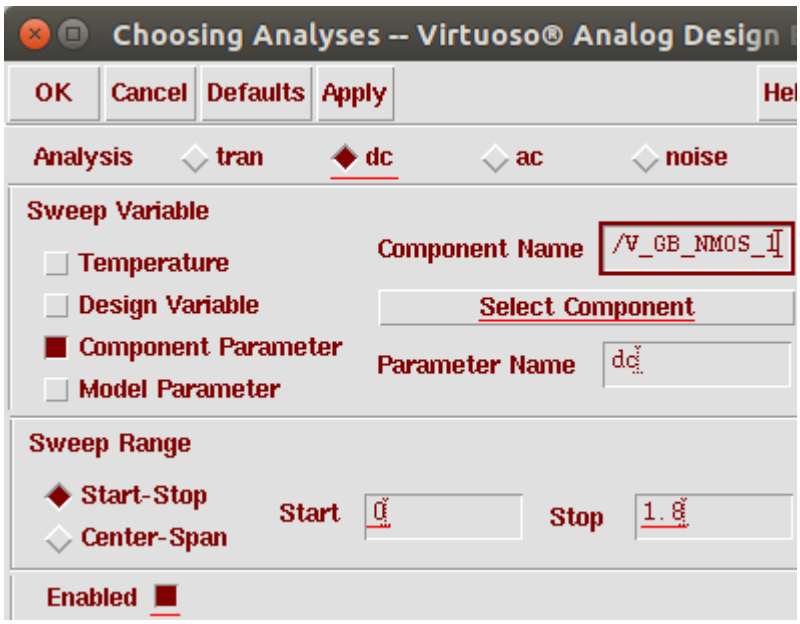
1/ Initialize as per Section 7.

2/ Only one circuit can be analyzed at a time, create the circuits as shown in Fig.5.1.

3/ To vary the gate voltage, go to:
Analyses → Choose ...

4/ The options should be as shown in the figure below: (also described in the next steps, 5 to 8)

FIG.8.2.1: CHOOSING ANALYSES



5/ Choose “dc”, then “Select Component”.

6/ Click on “Select Component”, click on the gate voltage part of the circuit to be tested.

7/ To vary the voltage from 0V to 1.8V[3], have “Start” = 0, “Stop” = 1.8.

8/ be sure the analysis is “Enabled”, then click on the “OK” button

3 The voltage range to be varied depends on the voltage limitations of the technology used.

SECTION 8.3) TECHNIQUE, I_{SQ}/V_T, CHOOSING OUTPUT:

1/ To monitor the current, do the following:
Outputs → To Be Plotted → Select On Schematic

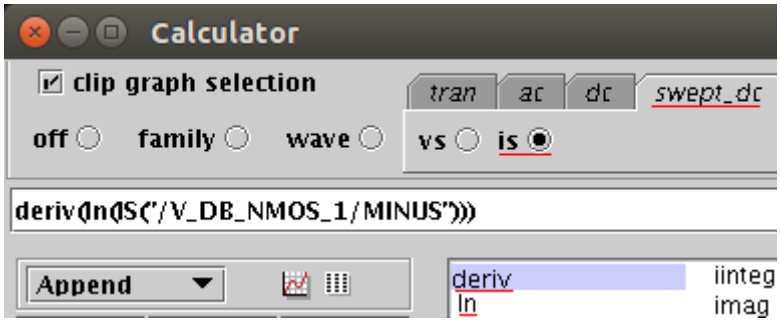
2/ To monitor the current, select the -'ve terminal of the drain-source voltage supply.[4]

3/ To do the transductance-to-drain current ratio (EQ.8.1), do the following:
Outputs → Setup

4/ Select “New Expression”, input a Name, then open the Calculator

5/ The result should be as shown in the figure below (all essentials underlined);
the “deriv” function does the derivative with respect to whatever is being swept (the gate voltage is being swept in this case).

FIG.8.3.1: GENERATING_OUTPUT



5/ Select “swept_dc”, “is”, select the -'ve terminal of the drain-source voltage supply.

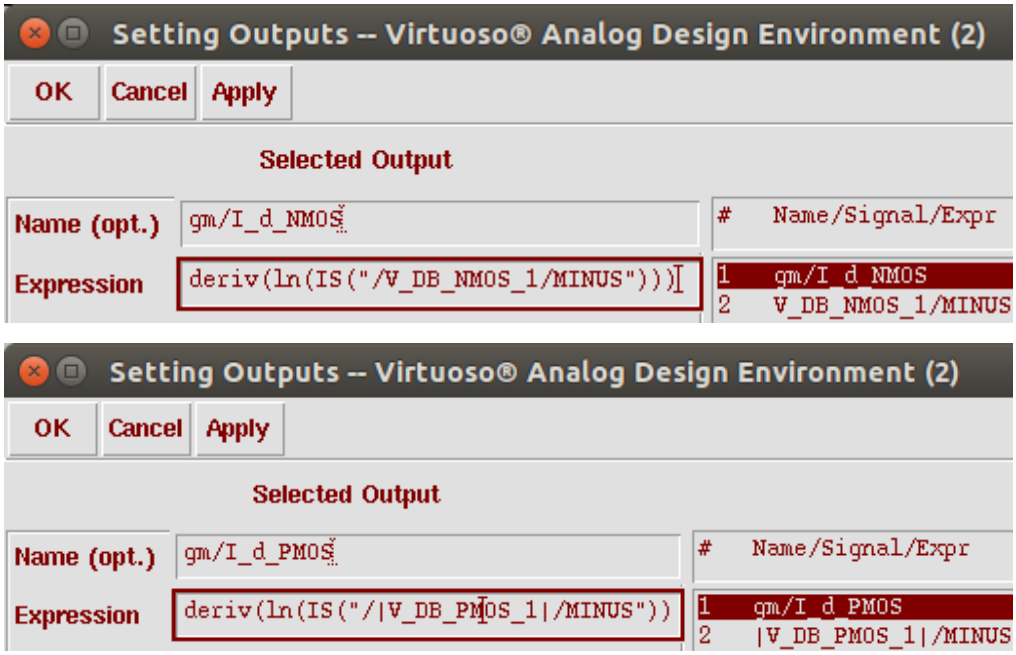
6/ Select “ln” to apply the natural logarithmic function to this current.

7/ Select “deriv” to allow the derivative (with respect to the swept variable) to be calculated.

4 Electrical current simulations under Cadence seem to work best when the terminal where electrons flow into is selected.

8/ The outputs should be setup as follows:

FIG. 8.3.2: I_{SQ} +V_{TH}, NMOS AND PMOS SETUP

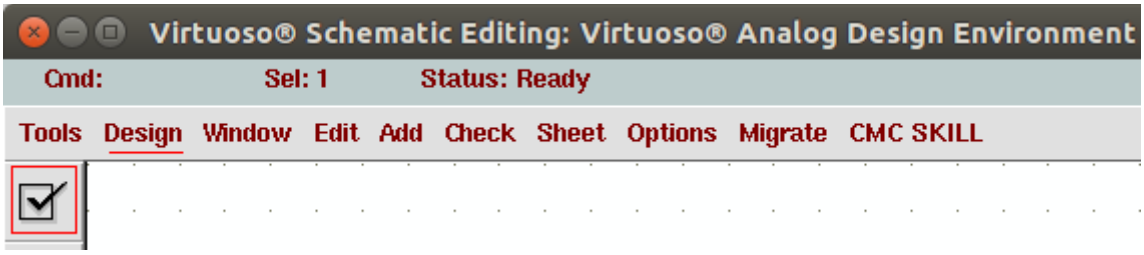


9/ Click OK.

SECTION 8.4) TECHNIQUE, I_{SQ}/V_T , RUNNING SIMULATION

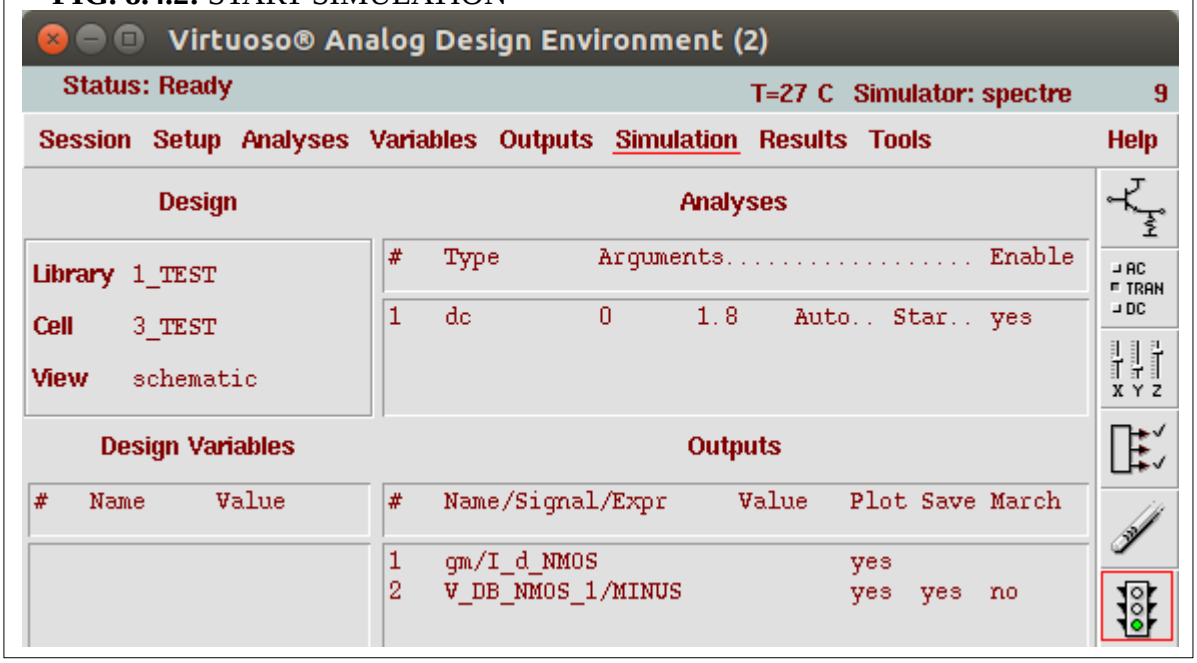
1/ Prior to the start of simulation, ensure the schematic has checked and saved, via the checkbox icon, or **Design → Check and Save** ,
as shown in the figure below:

FIG.8.4.1: SCHEMATIC CHECK AND SAVE



2/ Then on the simulator click on the greenlight icon, or **Simulation → Netlist and Run** as shown in the figure below:

FIG. 8.4.2: START SIMULATION



SECTION 8.5) TECHNIQUE, I_{SQ}/V_T , EXPECTED RESULTS

1/ The expected results should be as follows:

FIG.8.5.1: EXPECTED RESULTS I_{SQ} + V_T, NMOS

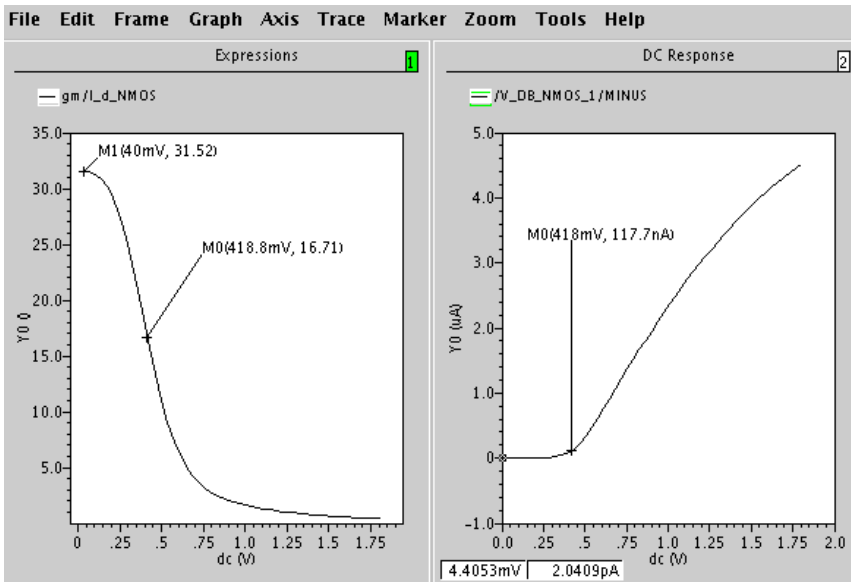
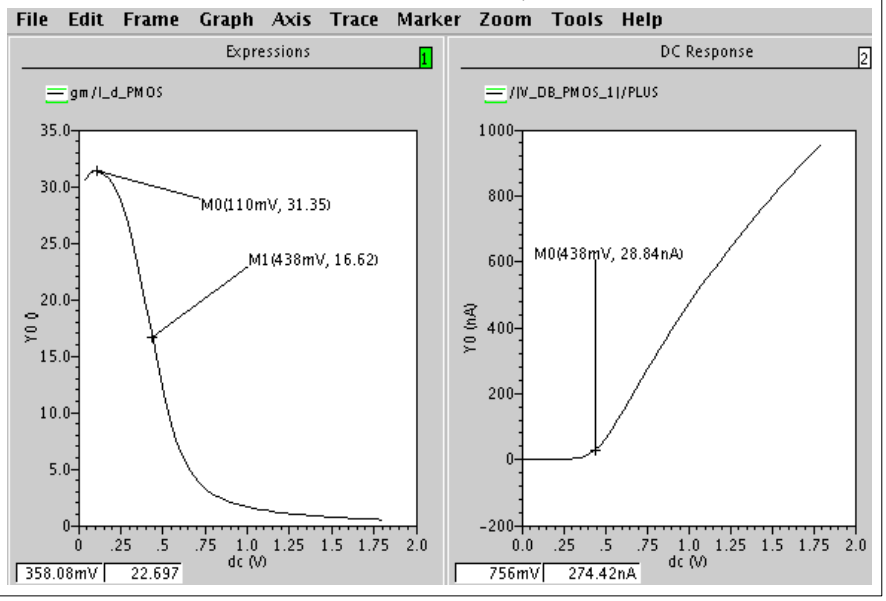


FIG.8.5.2: EXPECTED RESULTS I_{SQ} + V_T, PMOS



2/ In the simulation window that pops up, use "**Marker → Place → Trace Marker**" to find the maximum point of the g_m/I_D; the maximum point can be found adjusting the x values of the trace.

3/ Then put a trace on 53% of the maximum value of g_m/I_D; this can be done by adjusting the y values of the trace; The voltage at this 53% point corresponds to the **ACM threshold voltage**.

4/ On the drain current plot, put a trace corresponding to the ACM threshold voltage.
Here, the current, when divided by (0.885 * W/L), corresponds to the **sheet-specific current**.

SECTION 9) SIMULATION, SLOPE FACTOR

SECTION 9.1) TECHNIQUE, SLOPE FACTOR, BRIEF EXPLANATION

1/ For the slope factor circuits as shown in FIG.5.2, the source voltage is varied, while analysis of the gate voltage results in finding out the slope factor.

2/ Based on the condition that the drain current, I_D = 3 x (W/L) x I_{SQ}, the slope factor can be calculated as follows:

EQ.9.1:

$$n = \frac{d\,V_{GB}}{d\,V_{SB}}$$

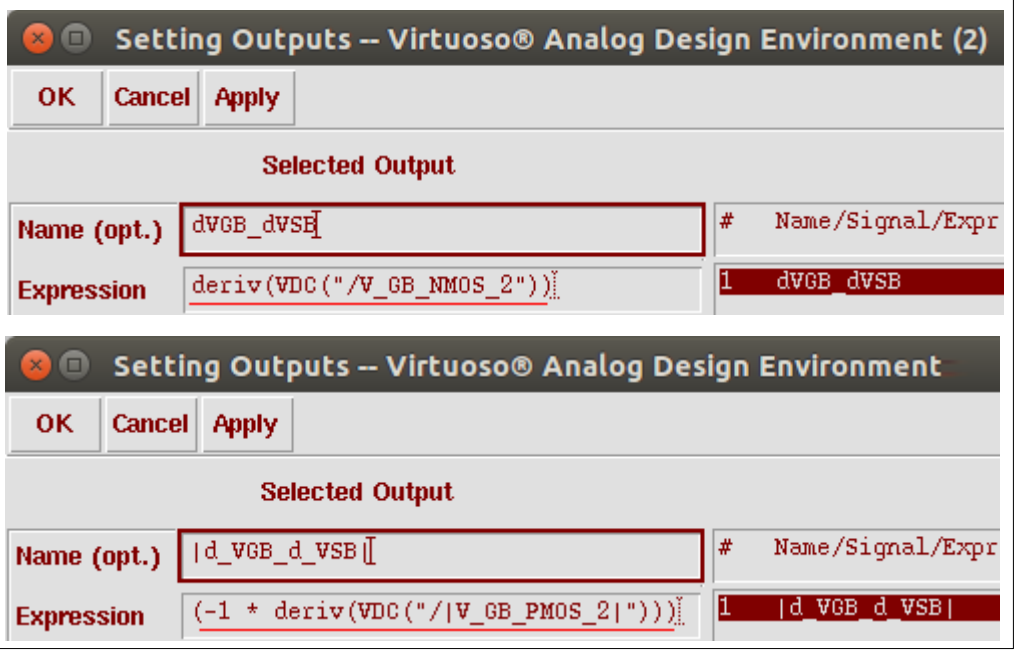
SECTION 9.2) TECHNIQUE, SLOPE FACTOR, CHOOSING ANALYSIS

1/ Initialize as per Section 7; create the circuits as shown in FIG.5.2.

2/ Have the setup similar to that shown in Section 8.2, but instead have the $|V_{SB}|$ voltage varied from 0V to 0.7V.

3/ Under the principles detailed in Section 8.3, setup the equations to accomplish EQ.9.1. The setup should be as follows:

FIG.9.2.1: SLOPE FACTOR, NMOS AND PMOS, SETUP



4/ Follow the same steps as shown in Section 8.4 to initialize and start the simulation.

SECTION 9.3) TECHNIQUE, SLOPE FACTOR, EXPECTED RESULTS

1/ The expected results should be as follows:

FIG.9.3.1: EXPECTED RESULTS, SLOPE FACTOR, NMOS

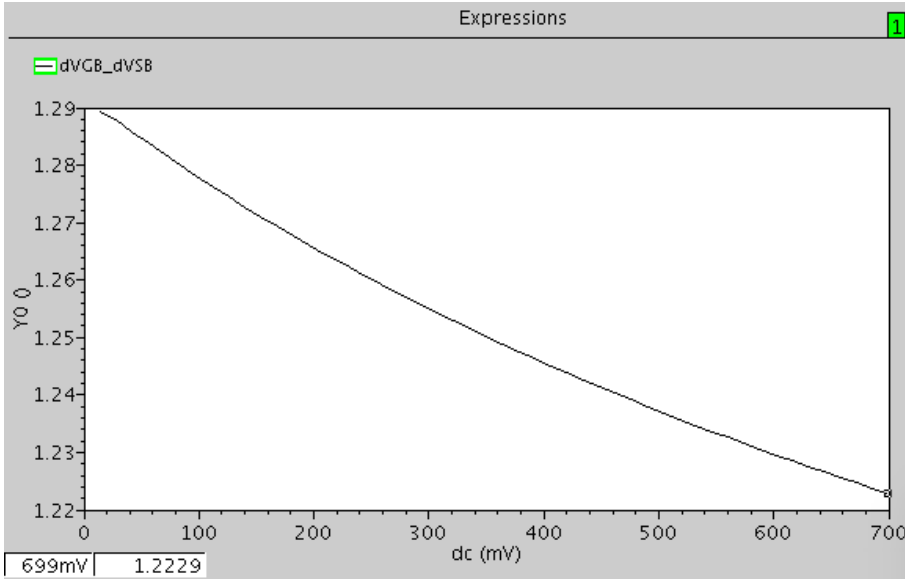
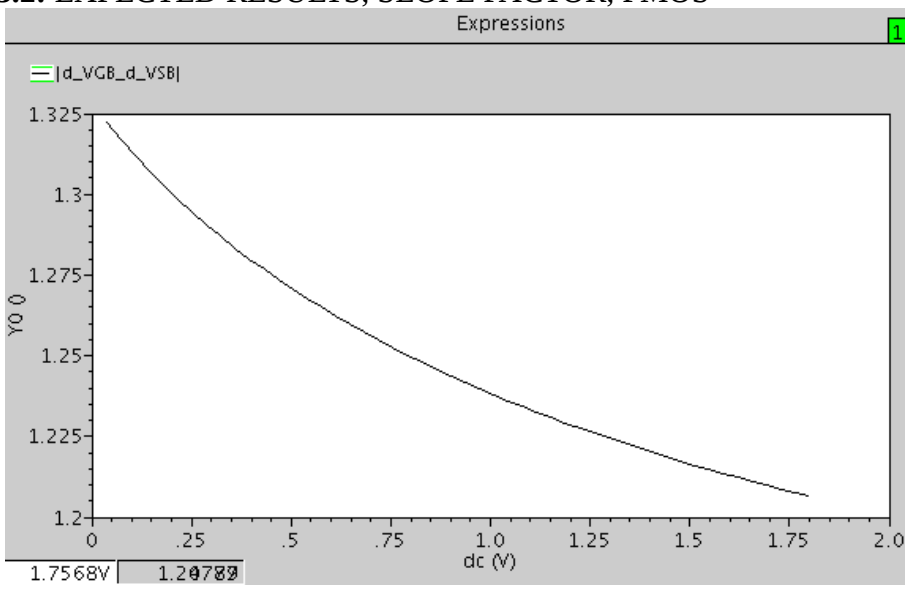


FIG.9.3.2: EXPECTED RESULTS, SLOPE FACTOR, PMOS



2/ The value of the **slope factor** should vary as $|V_{SB}|$ varies.

SECTION 10) SIMULATION, CHANNEL LENGTH MODULATION

SECTION 10.1) TECHNIQUE, CHANNEL LENGTH MODULATION, BRIEF EXPLANATION

1/ For the dL/dV$_{DS}$ circuits as shown in FIG.5.3, the drain voltage is varied, while analysis of the drain current results in finding out dL/dV$_{DS}$.

2/ The channel length modulation can be calculated as follows:

EQ.10.1:

$$\left|\frac{dL}{dV_{DS}}\right| = \frac{L_{EFF}}{\frac{\Delta V_{DS}}{\Delta I_D} I_D}$$

where
L$_{EFF}$ = effective channel length of the transistor (accounting for diffusion)
I$_D$ = the drain current at a particular value of V$_{DS}$

3/ The only unknown quantities of EQ.10.1 are ΔV$_{DS}$ and ΔI$_D$.

4/ Hence, simulation efforts will be directed at finding these unknowns.

SECTION 10.2) TECHNIQUE, CHANNEL LENGTH MOD., CHOOSING ANALYSIS:

1/ Initialize as per Section 7; create the circuits as shown in FIG.5.3.

2/ Have the setup similar to that shown in Section 8.2, but instead have the |V$_{DB}$| voltage varied from **0.3V to 1.6V.** The gate voltage is fixed to a value close to the intended inversion level (for this tutorial, you can make Vg=Vth, moderate inversion to get an average value). Note: the sweep range shown below only useful if you intend to use the model at with a similar (small) Vds. To extract a more generic parameter use the |V$_{DB}$| range suggested here and measure the average slope in the whole active range (keep in mind active range depends on inversion level).

3/ To monitor the current, select the -'ve terminal of the drain-source voltage supply.

4/ Follow the same steps as shown in Section 8.4 to initialize and start the simulation.

SECTION 10.3) TECHNIQUE, CHANNEL LENGTH MOD., EXPECTED RESULTS

1/ The expected results should be as follows:

FIG.10.3.1: EXPECTED RESULTS, SLOPE FACTOR, NMOS

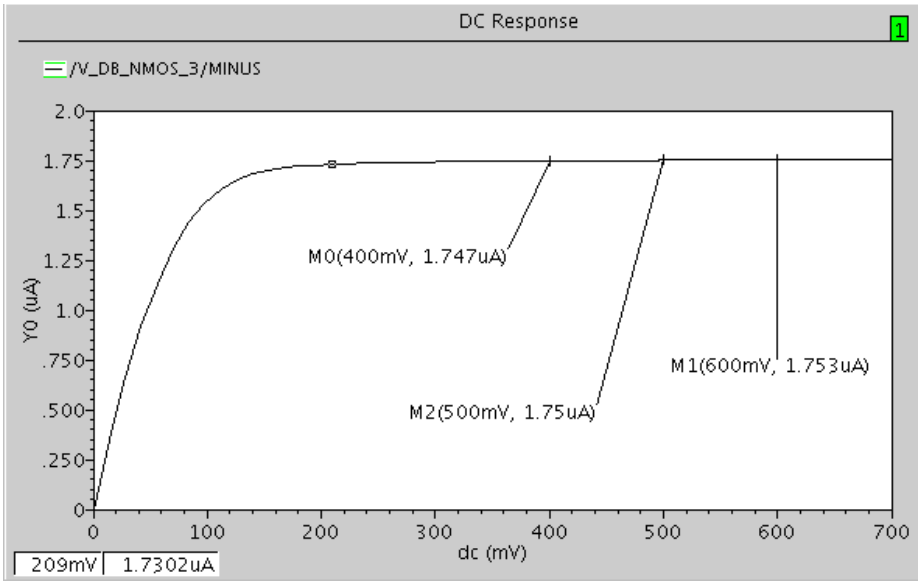
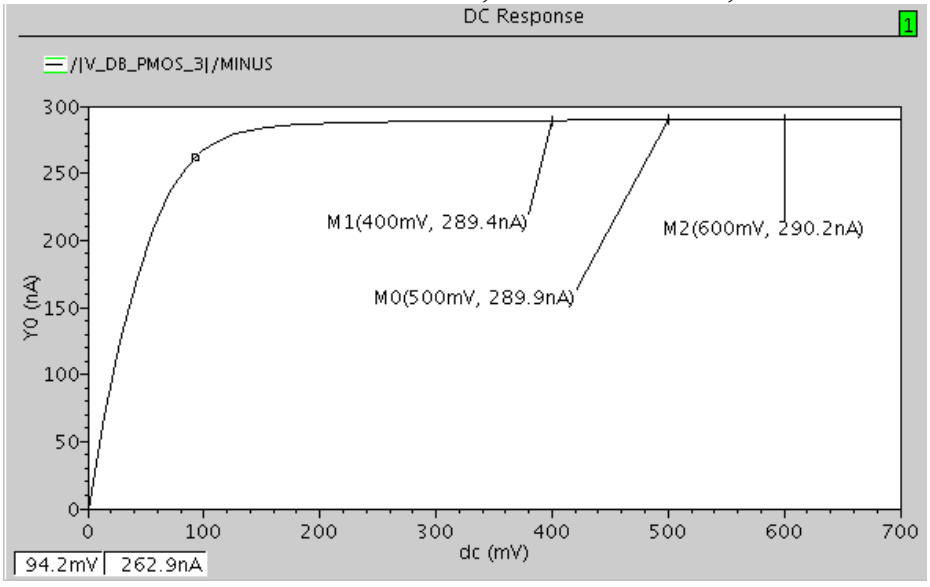


FIG.10.3.2: EXPECTED RESULTS, SLOPE FACTOR, PMOS



2/ Assuming $|V_{SB}| = 0V$, $|V_{DB}| = |V_{DS}|$; Apply a trace to the $|V_{DS}|$ of interest (in this case, 500 mV); at this $|V_{DS}|$ is the drain current (I_D from EQ. 10.1).

3/ Apply traces to +/- a certain increment of the $|V_{DS}|$ voltage (in this case, +/- 100 mV).

4/ The differences in voltage and current at these incremented points correspond to ΔV_{DS} and ΔI_D, hence, the **channel length modulation** can be calculated as per EQ.10.1.

SECTION 11) JUSTIFICATION OF I_{SQ} AND V_T EXTRACTION METHODS

SECTION 11.1) JUSTIFICATION, I_{SQ}

1/ The following is a justification of why at $|V_{GB}| = |V_T|$, the $I_{SQ} = I_D / (0.885 * W/L)$.

2/ The transistor voltages and inversion coefficients are related as follows:

EQ.11.1.1:

$$\frac{|V_{GB}| - |V_T|}{n\,V_{TH}} - \frac{|V_{SB(DB)}|}{V_{TH}} = F(i_{F(R)}) = \sqrt{1 + i_{F(R)}} - 2 + \mathrm{LN}\left(\sqrt{1 + i_{F(R)}} - 1\right)$$

3/ To accomplish the condition where $|V_{GB}|$ can = $|V_T|$, as many terms as possible are made to be zero, as aided by the following conditions:

EQ.11.1.2:

$$i_F = 3\ ;\ V_{SB} = 0\ \mathrm{V}$$

EQ.11.1.3:

$$\frac{|V_{GB}| - |V_T|}{n\,V_{TH}} = 0 = F(i_F = 3)$$

EQ.11.1.4:

$$|V_{GB}| = |V_T|$$

4/ Hence the forward inversion coefficient must be 3.

5/ With EQ. 11.1.3 simplifying the expression of EQ. 11.1.1, the reverse inversion coefficient is determined by having the drain-to-bulk voltage be fixed at a value that can cancel out the thermal voltage. In this case, the value is chosen to be half of the thermal voltage:

EQ.11.1.5:

$$|V_{DB}| = V_{TH}/2$$

EQ.11.1.6:

$$\frac{V_{TH}/2}{V_{TH}} = F(i_R) = \sqrt{1 + i_R} - 2 + \mathrm{LN}\left(\sqrt{1 + i_R} - 1\right)$$

6/ Based on the set value of the drain-to-bulk voltage, reverse inversion coefficient must be 2.115.

EQ.11.1.7:

$$\frac{1}{2} = F(i_R = 2.115)$$

7/ With i_F = 3 and i_R = 2.115, $|V_{GB}|= |V_T|$, $|V_{SB}|= 0$, $|V_{DB}|= V_{TH}/2$, then the sheet specific current can be computed:

EQ.11.1.8:

$$I_D = \frac{W}{L} I_{SQ} \left([i_F = 3] - [i_R = 2.115]\right) = \frac{W}{L} I_{SQ} \left(0.885\right)$$

EQ.11.1.9:

$$I_{SQ} = \frac{I_D}{\frac{W}{L} 0.885}$$

SECTION 11.2) JUSTIFICATION, 53% g_m/I_D , V_T

1/ The following justifies why 53% of the maximum transconductance-to-drain-current ratio correlates to the threshold voltage.

2/ The transconductance-to-current ratio starts off unknown, and hence the terms need to be solved.

EQ.11.2.1:

$$\frac{g_m}{I_D} = ?$$

3/ Transconductance is defined as the change in current in a transistor with respect to the change in a voltage at a given transistor terminal.

EQ. 11.2.2:

$$g_m = \frac{dI_D}{dV_{GB}}$$

4/ The drain current is defined as follows:

EQ. 11.2.3:

$$I_D = \frac{W}{L} I_{SQ} \left(i_F - i_R \right) \; ; \; i_{F(R)} = F(|V_{GB}|)$$

5/ As the inversion coefficients are a function of the gate voltage, the transconductance, therefore is expressed as:

EQ.11.2.4:

$$g_m = \frac{W}{L} I_{SQ} \left(\frac{di_F}{d|V_{GB}|} - \frac{di_R}{d|V_{GB}|} \right)$$

6/ To solve for the derivative of an inversion coefficient with respect to the gate voltage, the inversion coefficient function is first recalled and then rearranged to be expressed in terms of the gate voltage.

EQ.11.2.5:

$$F(i_{F(R)}) = \frac{|V_{GB}| - |V_T|}{nV_{TH}} - \frac{|V_{SB(DB)}|}{V_{TH}}$$

EQ.11.2.6:

$$|V_{GB}| = \left[\; F(i_{F(R)}) \; V_{TH} + |V_{SB(DB)}| \; \right] \; n \; + \; |V_T|$$

7/ The derivative of the gate voltage with respect to the inversion coefficient is calculated as follows:

EQ.11.2.7:

$$\frac{d|V_{GB}|}{di_{F(R)}} = \left[\frac{dF(i_{F(R)})}{di_{F(R)}} \; V_{TH} \right] \; n$$

EQ.11.2.8:

$$F(i_{F(R)}) = \sqrt{1 + i_{F(R)}} - 2 + \mathrm{LN}\left(\sqrt{1 + i_{F(R)}} - 1 \right)$$

EQ.11.2.9:

$$\frac{dF(i_{F(R)})}{di_{F(R)}} = \frac{dF(i_{F(R)})}{d\sqrt{1+i_{F(R)}}} \frac{d\sqrt{1+i_{F(R)}}}{di_{F(R)}} = \frac{1}{2} \frac{1}{\sqrt{1+i_{F(R)}}-1}$$

EQ.11.2.10:

$$\frac{d|V_{GB}|}{di_{F(R)}} = \left[\frac{1}{2} \frac{1}{\sqrt{1+i_{F(R)}}-1} V_{TH} \right] n$$

8/ Inverting the result from EQ.11.2.10 gets the derivative of the inversion coefficient with respect to the gate voltage, as required by EQ.11.2.4.

EQ.11.2.11:

$$\frac{di_{F(R)}}{d|V_{GB}|} = \left[2 \left(\sqrt{1+i_{F(R)}}-1\right) \frac{1}{V_{TH}} \right] \frac{1}{n}$$

9/ The transconductance then works out to be the following:

EQ.11.2.12:

$$g_m = \frac{W}{L} I_{SQ} \left(\sqrt{1+i_F}-\sqrt{1+i_R}\right) 2 \frac{1}{n\, V_{TH}}$$

10/ Combining transconductance with current, the transconductance-to-current ratio can be found.

EQ.11.2.13:

$$\frac{g_m}{I_D} = \frac{\frac{W}{L} I_{SQ}\, 2\, \frac{1}{n\, V_{TH}} (\sqrt{1+i_F}-\sqrt{1+i_R})}{\frac{W}{L} I_{SQ}\, (i_F - i_R)} \frac{\sqrt{1+i_F}+\sqrt{1+i_R}}{\sqrt{1+i_F}+\sqrt{1+i_R}}$$

EQ.11.2.14:

$$\frac{g_m}{I_D} = \frac{1}{n\, V_{TH}} \frac{2}{\sqrt{1+i_F}+\sqrt{1+i_R}}$$

11/ It is recognized that the maximum possible g_m/I_D is when the inversion coefficients → 0.

EQ.11.2.15:

$$\left[\frac{g_m}{I_D}\right]_{MAX} = \frac{1}{n\, V_{TH}}$$

12/ Based on the inversion coefficients for the conditions imposed from Section 11.1, the point at which $|V_{GB}| = |V_T|$ is 53% of the maximum g_m/I_D.

EQ.11.2.16:

$$\left[\frac{g_m}{I_D}\right]_{\substack{|V_{GB}|=|V_T| \\ |V_{DB}|=\frac{1}{2}V_{TH}}} = \left[\frac{g_m}{I_D}\right]_{MAX} \left(\frac{2}{\sqrt{1+3}+\sqrt{1+2.115}}\right) \cong 0.53 \left[\frac{g_m}{I_D}\right]_{MAX}$$

SECTION 12) JUSTIFICATION OF SLOPE FACTOR EXTRACTION METHOD

SECTION 12.1) JUSTIFICATION, ID = 3*(W/L)*ISQ

1/ As the circuits of FIG.5.2 are diode-connected, the circuits are forward-biased, resulting in $i_F >> i_R$.

EQ.12.1.1:

$$I_D \cong \frac{W}{L} I_{SQ}\, i_F$$

2/ With W = L, and having 3 times the drain current, a condition is forced that allows $i_F = 3$.

EQ.12.1.2:

$$3\, I_D \cong I_{SQ}\, i_F \;;\; \therefore i_F = 3$$

EQ.12.1.3:

$$F(i_F = 3) = \sqrt{1+3} - 2 + \mathrm{LN}\left(\sqrt{1+3} - 1\right) = 0$$

3/ Based on $i_F = 3$, then the following simplifications apply.

EQ.12.1.4:

$$F(i_F) = 0 = \frac{|V_{GB}| - |V_T|}{n\, V_{TH}} - \frac{|V_{SB}|}{V_{TH}}$$

EQ.12.1.5:

$$\frac{|V_{GB}| - |V_T|}{n} - |V_{SB}| = 0$$

EQ.12.1.6:

$$n\, |V_{SB}| = |V_{GB}| - |V_T|$$

4/ To isolate the slope factor, n, the derivative is taken on both sides of EQ. 12.1.6:

EQ.12.1.7:

$$\frac{dn|V_{SB}|}{d|V_{SB}|} = \frac{d|V_{GB}|}{d|V_{SB}|} - \frac{d|V_T|}{d|V_{SB}|}$$

EQ.12.1.8:

$$n = \frac{d|V_{GB}|}{d|V_{SB}|} - 0$$

SECTION 13) JUSTIFICATION OF CHAN. LENGTH MOD. EXTRACTION METHOD

1/ The channel length modulation is based on the definition of the output resistance, r_o:

EQ.13.1.1:

$$\frac{\Delta V_{DS}}{\Delta I_D} = r_o = \frac{1}{\lambda}\frac{1}{I_D} = \frac{L_{EFF}}{\left|\frac{\partial L}{\partial V_{DS}}\right|}\frac{1}{I_D}$$

2/ Rearranging EQ.13.1.1 results in an expression for the channel length modulation.

EQ.13.1.2:

$$\left|\frac{\partial L}{\partial V_{DS}}\right| = \frac{L_{EFF}}{\frac{\Delta V_{DS}}{\Delta I_D}}\frac{1}{I_D}$$

SECTION 14) EQUATION SOURCE CODE

1/ Equations were made with a Latex-based editor, the source code is as follows:

EQ.2.1:
I_D = \frac{W}{L} I_{SQ} \left(i_F - i_R \right)
EQ.2.2:
I_{SQ} = \frac{1}{2} \; n \; \mu \; C_{OX} \; {V_{TH}}^2
EQ.2.3:
F(i_{F(R)}) = \sqrt{1+i_{F(R)}} \; - \;2 \; + \;\textup{LN} \left(\sqrt{1+i_{F(R)}} -1 \right)
EQ.2.4:
F(i_{F(R)}) = \frac{ |V_{GB}| - |V_{T}| }{n V_{TH}} - frac{| V_{SB(DB)}|}{V_{TH}}
EQ.8.1:
\frac{g_m}{I_D} =
\frac {\frac{dI_D}{dV_{GB}}}{I_D}
= \frac{d\;\textup{LN}(I_D)}{d\;V_{GB}}
EQ.9.1:
n = \frac{d\;V_{GB}}{d\;V_{SB}}
EQ.10.1:
\left| \frac{dL}{dV_{DS}} \right| = \frac{L_{EFF}}{ \frac{\Delta V_{DS}}{\Delta I_D} {I_D} }
EQ.11.1.1:
\frac{|V_{GB}| - |V_T|}{ n \; V_{TH}} -
\frac{|V_{SB(DB)}|}{V_{TH}} =
F(i_{F(R)}) =
\sqrt{1+i_{F(R)}} \; - \;2 \; + \;\textup{LN} \left(\sqrt{1+i_{F(R)}} -1 \right)
EQ.11.1.2
i_F = 3 \; ; \; V_{SB} = 0\; \textup{V}
EQ.11.1.3
\frac{|V_{GB}| - |V_T|}{ n \; V_{TH}}
= 0 = F(i_F = 3)
EQ.11.1.4
|V_{GB}| = |V_T|
EQ.11.1.5
|V_{DB}| = V_{TH} / 2
EQ.11.1.6
\frac{V_{TH} / 2}{V_{TH}}
= F(i_R) =
\sqrt{1+i_{R}} \; - \;2 \; + \;\textup{LN} \left(\sqrt{1+i_{R}} -1 \right)
EQ.11.1.7
\frac{1}{2} = F(i_R = 2.115)
EQ.11.1.8
I_D = \frac{W}{L} I_{SQ} \left([i_F = 3] - [i_R = 2.115] \right) =
\frac{W}{L} I_{SQ} \left(0.885 \right)
EQ.11.1.9
I_{SQ} = \frac{I_D}{\frac{W}{L} \; 0.885}
EQ.11.2.1:
\frac{g_m}{I_D} = ?
EQ. 11.2.2:
g_m = \frac{dI_D}{d|V_{GB}|}
EQ. 11.2.3:
I_D = \frac{W}{L} I_{SQ} \left(i_F - i_R \right)\; ; \; i_{F(R)} = F(|V_{GB}|)
EQ.11.2.4:
g_m = \frac{W}{L} I_{SQ} \left(\frac{di_F}{d|V_{GB}|} - \frac{di_R}{d|V_{GB}|} \right)
EQ.11.2.5:
F(i_{F(R)}) = \frac{ |V_{GB}| - |V_{T}| }{n \; V_{TH}} - \frac{| V_{SB(DB)}|}{V_{TH}}
EQ.11.2.6:
|V_{GB}| =
\left[\;
F(i_{F(R)}) \; V_{TH} + |V_{SB(DB)}|
\; \right]
\; n \; + \; |V_{T}|
EQ.11.2.7:
\frac{d|V_{GB}|}{di_{F(R)}} =
\left[\;
\frac{dF(i_{F(R)})}{di_{F(R)}} \; V_{TH}
\; \right]
\; n
EQ.11.2.8:
F(i_{F(R)}) = \sqrt{1+i_{F(R)}} \; - \;2 \; + \;\textup{LN} \left(\sqrt{1+i_{F(R)}} -1 \right)
EQ.11.2.9:
\frac{dF(i_{F(R)})}{di_{F(R)}} =
\frac{dF(i_{F(R)})}{d \sqrt{1+i_{F(R)}}} \;
\frac{d \sqrt{1+i_{F(R)}} }{di_{F(R)} }
= \frac{1}{2} \;
\frac{1}{ \sqrt{1+i_{F(R)}}-1}
EQ.11.2.10:
\frac{d|V_{GB}|}{di_{F(R)}} =
\left[\;
\frac{1}{2} \;\frac{1}{ \sqrt{1+i_{F(R)}}-1} \; V_{TH}
\; \right]
\; n
EQ.11.2.11:
\frac{di_{F(R)}}{d|V_{GB}|} =
\left[\;
2 \; \left(\sqrt{1+i_{F(R)}}-1 \right)
\; \frac{1}{V_{TH} }
\; \right]
\; \frac{1}{n}
EQ.11.2.12:
g_m = \frac{W}{L} I_{SQ}
\left(
\sqrt{1+i_F} - \sqrt{1+i_R}
\right) \;
2 \; \frac{1}{n \; V_{TH}}
EQ.11.2.13:
\frac{g_m}{I_D} =
\frac
{
  \frac{W}{L} I_{SQ} \;
  2 \; \frac{1}{n \; V_{TH}}
  \left(
    \sqrt{1+i_F} - \sqrt{1+i_R}
  \right)
}
{\frac{W}{L} I_{SQ} \; (i_F - i_R)}
\;
\frac
{ \sqrt{1+i_F} + \sqrt{1+i_R} }
{ \sqrt{1+i_F} + \sqrt{1+i_R} }
EQ.11.2.14:
\frac{g_m}{I_D} =
\frac{1}{n \; V_{TH}} \;
\frac
{2}
{\sqrt{1+i_F} + \sqrt{1+i_R}}
EQ.11.2.15:

\left[
\frac{g_m}{I_D}
\right]_{MAX} =
\frac{1}{n \; V_{TH}}

EQ.11.2.16:

\left[
\frac{g_m}{I_D}
\right]_{|V_{GB}| = |V_T| \atop |V_{DB}| = \frac{1}{2}\;V_{TH} } =
\left[
\frac{g_m}{I_D}
\right]_{MAX}
\left(
  \frac{2}{\sqrt{1+3} + \sqrt{1+2.115}}
\right)
\cong
0.53\left[
\frac{g_m}{I_D}
\right]_{MAX}

EQ.12.1.1:

I_D \cong \frac{W}{L} I_{SQ} \; i_F

EQ.12.1.2:

3 \; I_D \cong I_{SQ} \; i_F \; ; \; \therefore i_F = 3

EQ.12.1.3:

F(i_{F} = 3) = \sqrt{1+3} \; - \;2 \; + \;\textup{LN} \left(\sqrt{1+3} -1
\right)
 = 0

EQ.12.1.4:

F(i_{F})= 0 = \frac{ |V_{GB}| - |V_{T}| }{n \; V_{TH}} - \frac{|
V_{SB}|}{V_{TH}}

EQ.12.1.5:

\frac{ |V_{GB}| - |V_{T}| }{n} - |V_{SB}| = 0

EQ.12.1.6:

n \; |V_{SB}| = |V_{GB}| - |V_{T}|

EQ.12.1.7:

\frac{d n|V_{SB}|}{d|V_{SB}|} = \frac{d|V_{GB}|}{d|V_{SB}|} -
\frac{d|V_{T}|}{d|V_{SB}|}

EQ.12.1.8:

n= \frac{d|V_{GB}|}{d|V_{SB}|} - 0

EQ.13.1.1:

\frac{\Delta V_{DS}}{ \Delta I_D} =
r_o = \frac{1}{\lambda} \; \frac{1}{I_D} =
\frac
{L_{EFF}}
{ \left| \frac{ \partial L }{ \partial V_{DS} } \right| }
\; \frac{1}{I_D}

EQ.13.1.2:

\left| \frac{ \partial L }{ \partial V_{DS} } \right| =
\frac
{L_{EFF}}
{\frac{\Delta V_{DS}}{ \Delta I_D}}
\;
\frac{1}{I_D}

SECTION 15) REFERENCES

[1] P. Luong, “Sub-1 V, 4 nA CMOS voltage references with digitally-trimmable temperature coefficient,” M.Sc.Eng. Thesis, Lakehead University: Ontario, Canada, 2014. Retrieved from http://knowledgecommons.lakeheadu.ca/handle/2453/578

[2] M.C. Schneider and C. Galup-Montoro, CMOS Analog Design Using All-Region MOSFET Modeling, New York, Cambridge University Press, 2010.