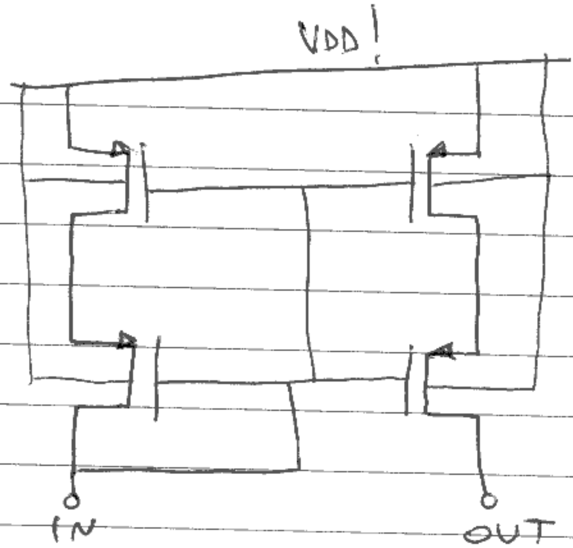
1)

(+5)



PMOS
SUBSTRATE
LABELED NODES
METAL 1
TOPOLOGY

(+5) 2)

$L = 0.2\mu m$
$W = 0.6\mu m$

(+1) { Leff ACTIVE REGION JUST.

(STRONG INV) $\simeq \sqrt{i_{f1}}$

$V_{in} = 1.1V \Rightarrow$ NMOS: $\frac{1.1V - 0.39V}{1.3} = V_T\,\underbrace{F(i_{f1})}_{\simeq\sqrt{i_{f1}}}$

~0.09V MODERATE $\quad i_{f1} = 441$ (+1)

$\therefore I_D = 182$ nA (NMOS) (CONSIDERING Leff)

PMOS: $\frac{\overbrace{(1.6V - 1.1V)}^{0.5V} - 0.41V}{1.3} = V_T\,\underbrace{F(i_{f2})}_{=2.663}$

$i_{f2} \simeq 13$ FROM GRAPH (+2) { (+1) (+1) MODEL

SINCE $I_{D_N} = I_{D_P} \longrightarrow$

$I_{SQn}\left(\frac{W}{L_{eff}}\right)_n i_{f1} = I_{SQp}\left(\frac{W}{L_{eff}}\right)_p i_{f2}$

$W_P = \frac{I_{SQn}\, i_{f1} W_n}{I_{SQp}\, i_{f2}} \;\; \boxed{64\mu m}$

(+1) RES

$\boxed{64\mu m}$

CONSIDERING L OR $L_{eff} = L - 2L_D$ MAKES NO DIFFERENCE FOR THIS PROBLEM, BUT IF L IS USED FOR ANY CALCULATION, L_D SHOULD BE CONSIDERED SINCE L IS SMALL.

$V_{G1} = 0.339V$

3) a) $\cancel{\text{xxx}}$ $i_{f_2} = i_{f_1}$ (SAME V_G, V_S, V_B)

$$i_{f_2} = \frac{5\mu A}{I_S} = 0.974$$

$I_S \leftarrow I_{S_1} = I_{S_2} = I_{S_3} = I_S$

$i_{r_2} = i_{f_3}$ (SAME V_G, V_B AND $V_{S_3} = V_{D_2}$)

(1) $I_{OUT} = I_S\, i_{f_3}$ (i_{r_3} NEGLIGIBLE, ASSUMING $V_{DS_3} > V_{DS_3\,SAT}$)

(2) $I_{OUT} = I_S\left(i_{f_2} - \underbrace{i_{f_3}}_{=i_{r_2}}\right)$ (+2) DERIV

FROM (1) AND (2): (+3) RESULTS

$$\cancel{I_S}\, i_{f_3} = \cancel{I_S}\left(i_{f_2} - i_{f_3}\right)$$

$$2\, i_{f_3} = i_{f_2}$$

$$i_{f_3} = \frac{i_{f_2}}{2} = 0.487$$

CHECK $V_{DS_3} > V_{DS_{SAT_3}} = V_T\left(3 + \sqrt{1.487}\right) = 0.110V$

$$\frac{V_G - V_{th}}{n} - V_{D_2} = V_T\, q(0.487) \quad (M3)$$

$$\frac{V_G - V_{th}}{n} = V_T\, q(0.974) \quad (M2)$$

$$\therefore V_{D_2} = V_T\left[q(0.974) - q(0.487)\right] = 0.021V$$

$\therefore V_{DS_3} \cong 1V \gg V_{DS_{SAT_3}}$ ASSUMPTION CORRECT

b) $I_{OUT} = 2.5\mu A \quad \left(= \frac{I_{in}}{2}\right)$ (+2)

c) METHOD 1 : $V_{OUT\,MIN} = \underbrace{0.021\,V}_{=V_{D2}} + \underbrace{V_{DSAT_3}}_{=0.110V} = \boxed{0.131V}$

METHOD 2 :

(M3 − M2) EQUIVALENT TO A LONGER-CHANNEL TRANSISTOR WITH

(+3) {(+1) IF REASONABLE; (+2) CORRECT. $\quad i_f = i_{f_1}$

$$V_{OUT\,min} = V_T\left(3 + \sqrt{1.974}\right) = \boxed{0.115\,V}$$

d) $r_o = \frac{V_A}{I_{OUT}}$

FOR EQUIVALENT TRANSISTOR, $V_A = \frac{3\mu m}{0.05\frac{\mu m}{V}} = 60V$

$$\frac{\Delta I}{I_{OUT}} = \frac{\Delta V}{I_{OUT} r_o} = \frac{\Delta V}{V_A} = \boxed{1.66\,\%}$$

(+3) {(+1) IF 'SOMEWHAT REASONABLE'

4) a) $\left|V_{DSSAT_5}\right| = 0.397\,V$ (+2) DERIVATION (+1) LOGIC

VOLTAGES REFERRED TO VDD : (USING ABSOLUTE VALUES)

$$\frac{V_{G1} - V_{th}}{n} - \underbrace{V_{S1}}_{=V_{DSSAT5}} = V_T\,\underbrace{f(i_{f1})}_{=3.86} \qquad (1)$$

$$V_{G1} = 1.06V$$

(+1) RESULT

$$\therefore V_{CM\,MAX} = 1.8V - 1.06V = \boxed{0.74V}$$

b) $\left|V_{G1}\right| = 1.8V - 0.2V = 1.6V$

USING (1) → FIND $V_{S1} = 0.815V$ (+2) DERIV

REFERRED TO GND $\rightarrow$ $V_{S_1} = 1.8V - 0.815V$
$= 0.985V$ (+1) LOGIC

$$V_{OUT\ MAX} = \underbrace{V_{S_1}}_{0.985V} - \underbrace{\boxed{V_{DSSAT_2}}}_{0.197V} = \boxed{0.788\ V}$$ (+1) RESULT

c) $$I_{BIAS} = \underbrace{C}_{0.5pf} \cdot \underbrace{\frac{dV}{dt}}_{2000\frac{V}{\mu s}} = 100\mu A$$ (+2)

$$W_5 = \frac{100\mu A \times 2\mu m}{I_{sep}\ i_{f5}} = \boxed{38\mu m}$$ (+1)

$$W_1 = W_2 = \frac{50\mu A \times 2\mu m}{I_{sop}\ i_{f2}} = \boxed{14.28\mu m}$$ (+1)

$$W_3 = W_4 = \frac{50\mu A \times 2\mu m}{I_{sqn}\ i_{f3}} = \boxed{11.3\mu m}$$ (+1)