ENGI 5131 --- Tutorial 4

Layout vs. Schematic and Extracted View Simulation

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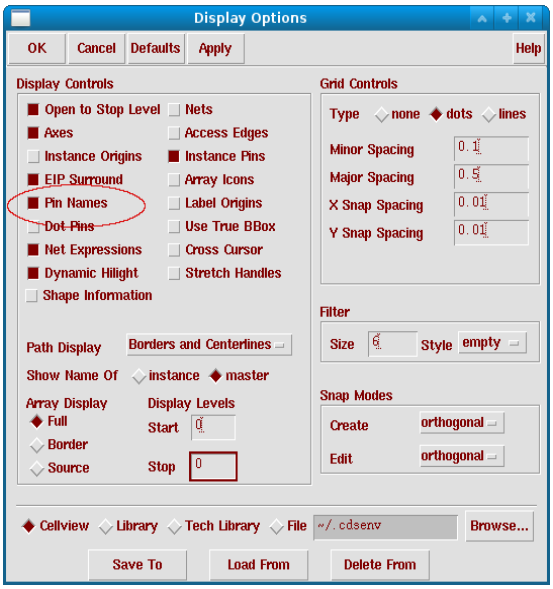
Objective

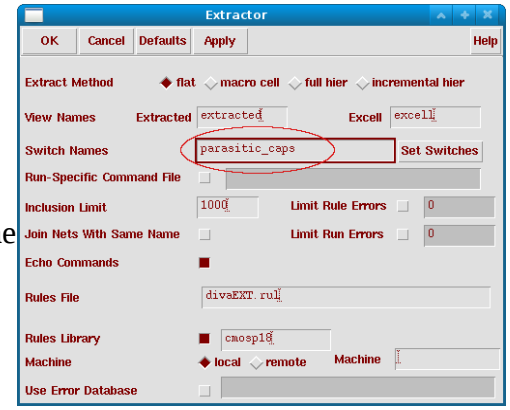
To simulate a circuit with extracted parasitic from a layout and perform post-layout simulation.

Open the inverter layout that you have created in the last tutorial. If the pin names (**vdd!, gnd!, in, out**) are not visible in the layout view, click **Option → Display Options** and select the **Pin Names** button in the **display controls** box. Save it.



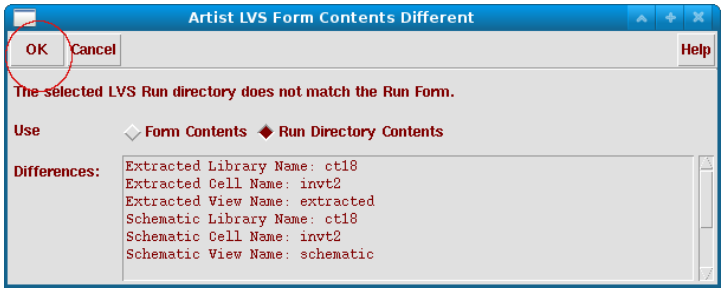
Extracting circuit from a layout

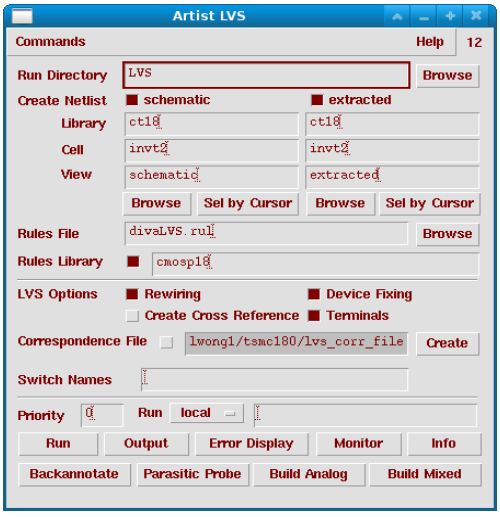
We are going to extract the parasitic capacitor from our layout for post layout simulation. In the Layout Editor menu, click **Verify → Extract**. The extractor window will pop up. Click the **set switches** button and select **parasitic_caps**.

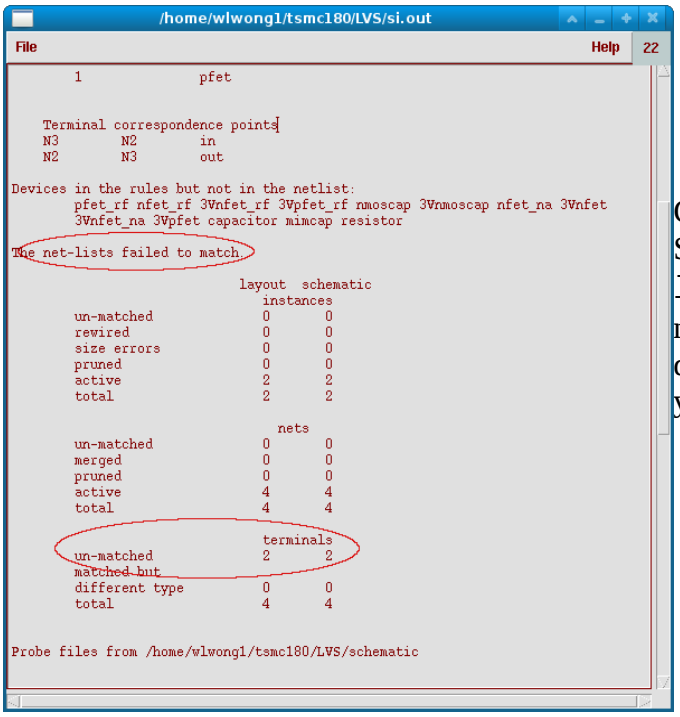


Layout Versus Schematic

In the Layout Editor menu, click **Verify → LVS → OK.** Click the **Run** button and wait for LVS to finish.

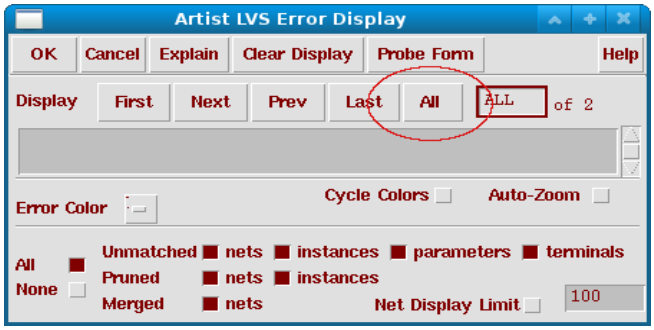


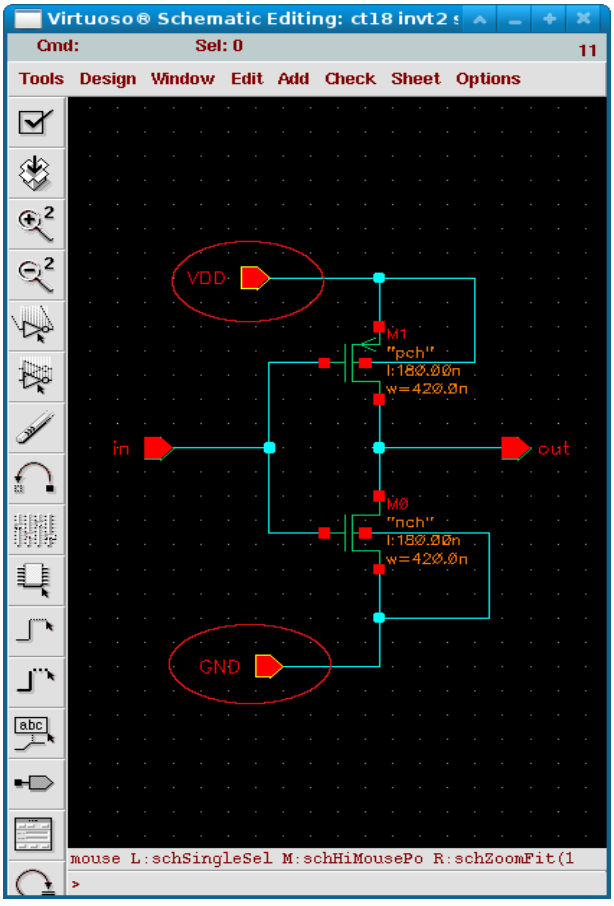




Click the **Output** button to display the report. Scroll down and look for the line "`The net-lists failed to match`" to verify there is no mismatch between the layout and schematic diagram. But if you follow the tutorial closely, you should find two errors in the report.

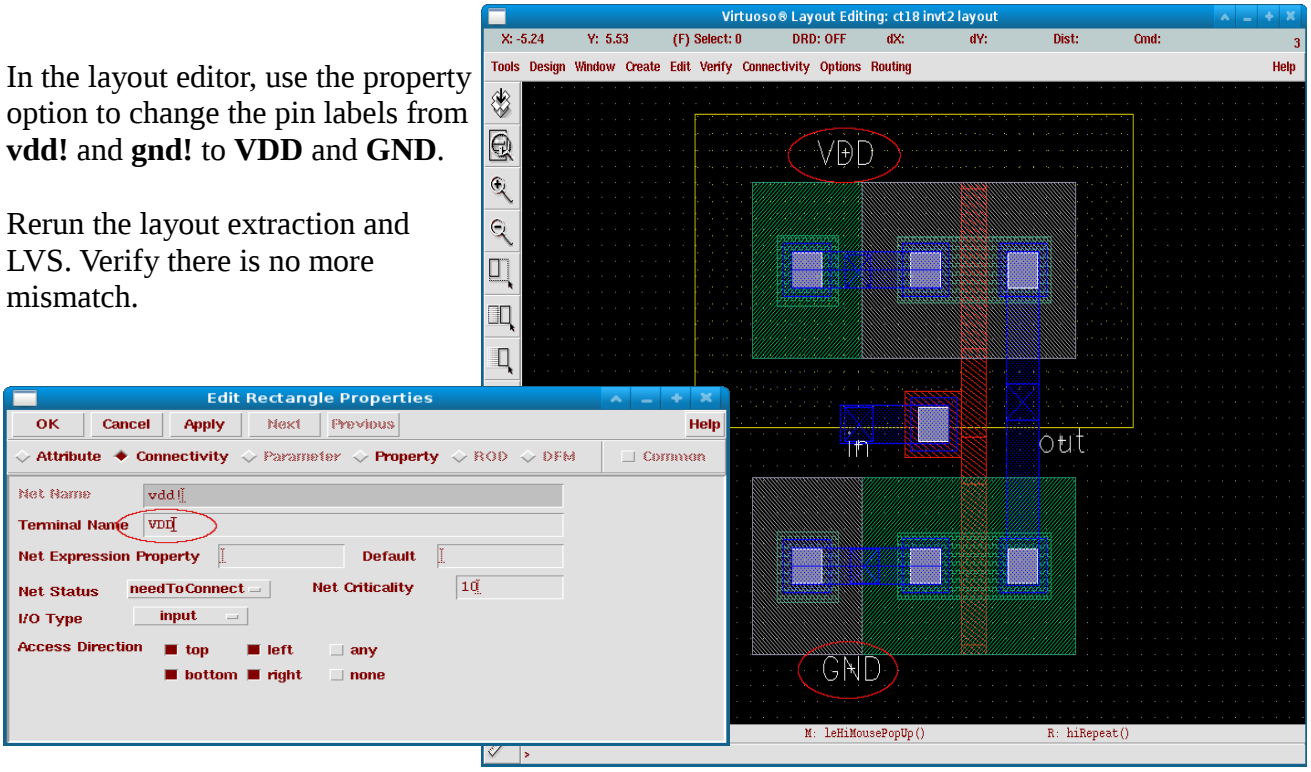
To locate errors in the schematic diagram, open the schematic of the inverter; return to the Artist LVS window and click "**Error Display**". The mismatched items will be highlighted in the schematic editor.





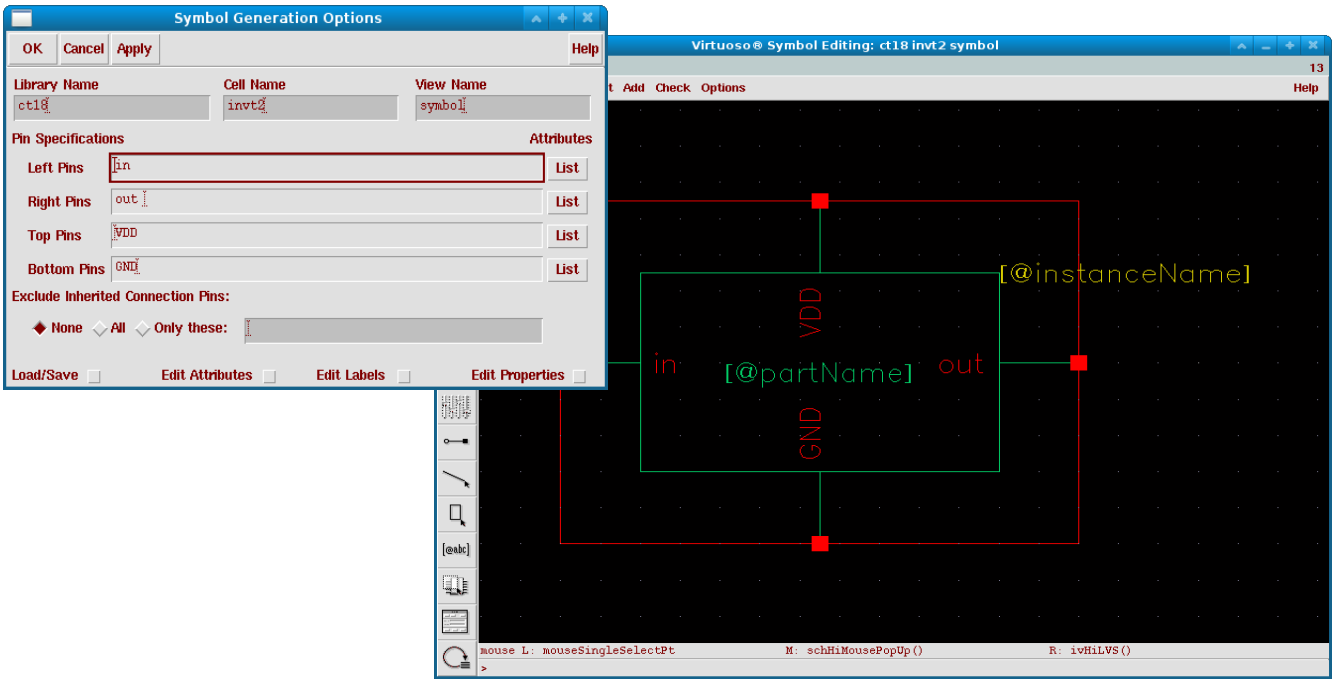
In the layout editor, use the property option to change the pin labels from **vdd!** and **gnd!** to **VDD** and **GND**.

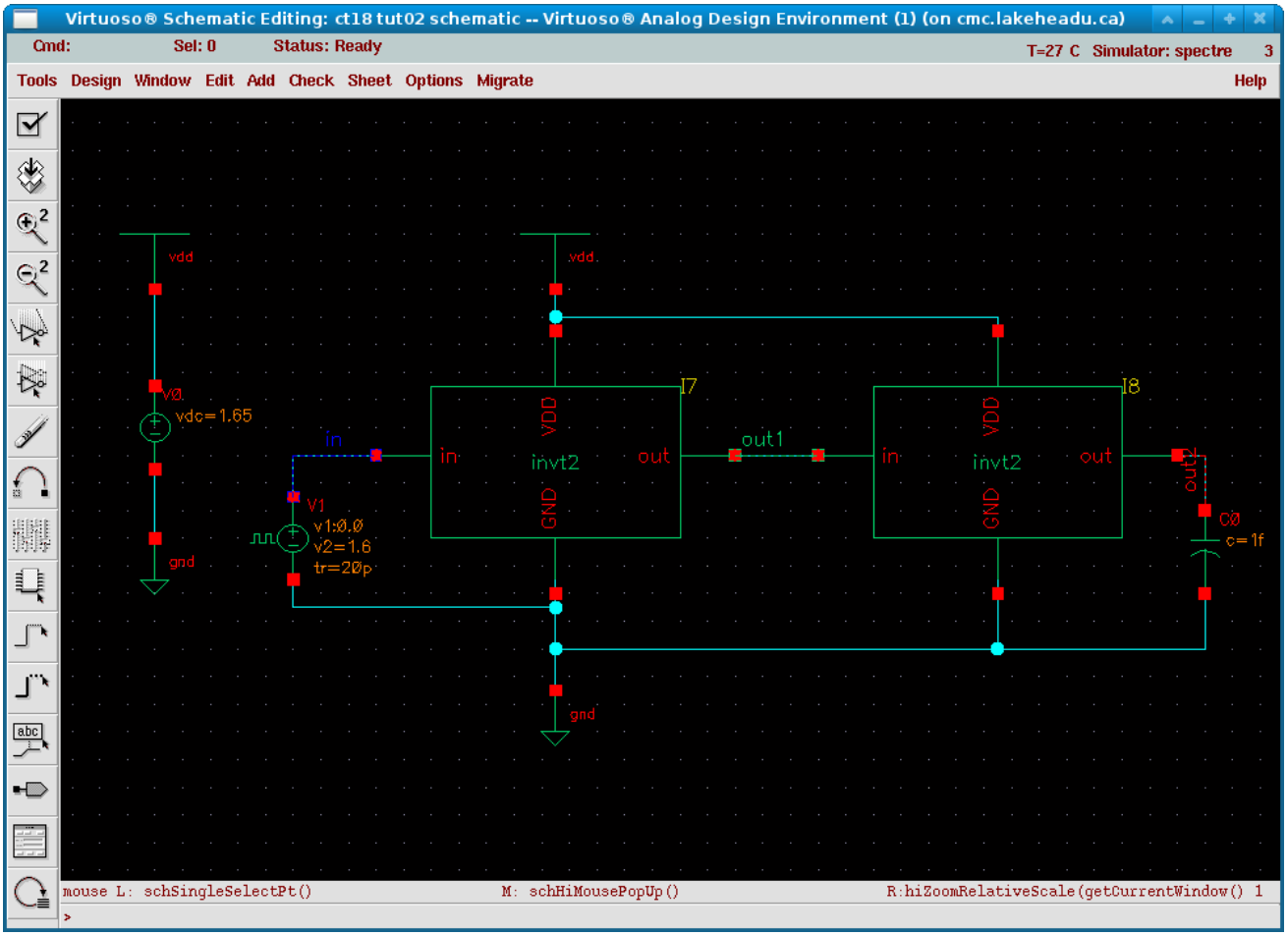
Rerun the layout extraction and LVS. Verify there is no more mismatch.



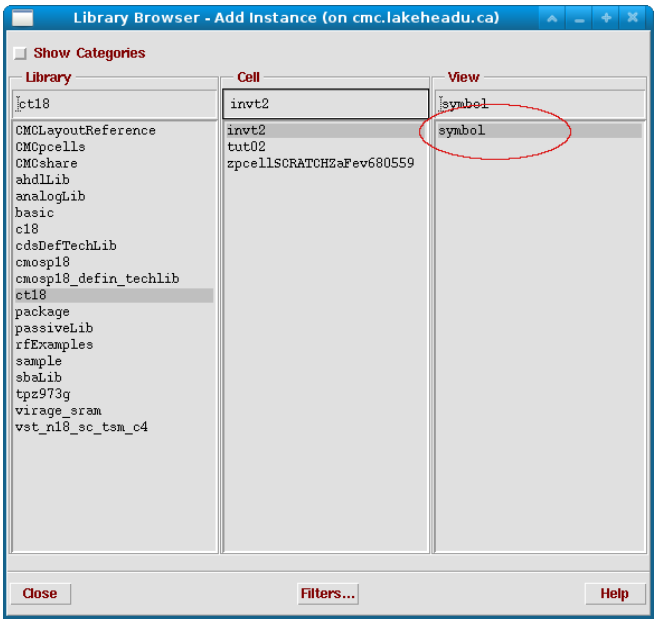
Creating symbols

On the menu bar of the schematic editor, click **Design → Create Cellview → From Cellview → OK.** In the **Symbol Generation Options** window, rearrange "**Pin Specifications**" as shown in the figures below. Click **OK** to continue. Save it and close the Symbol Editor window.

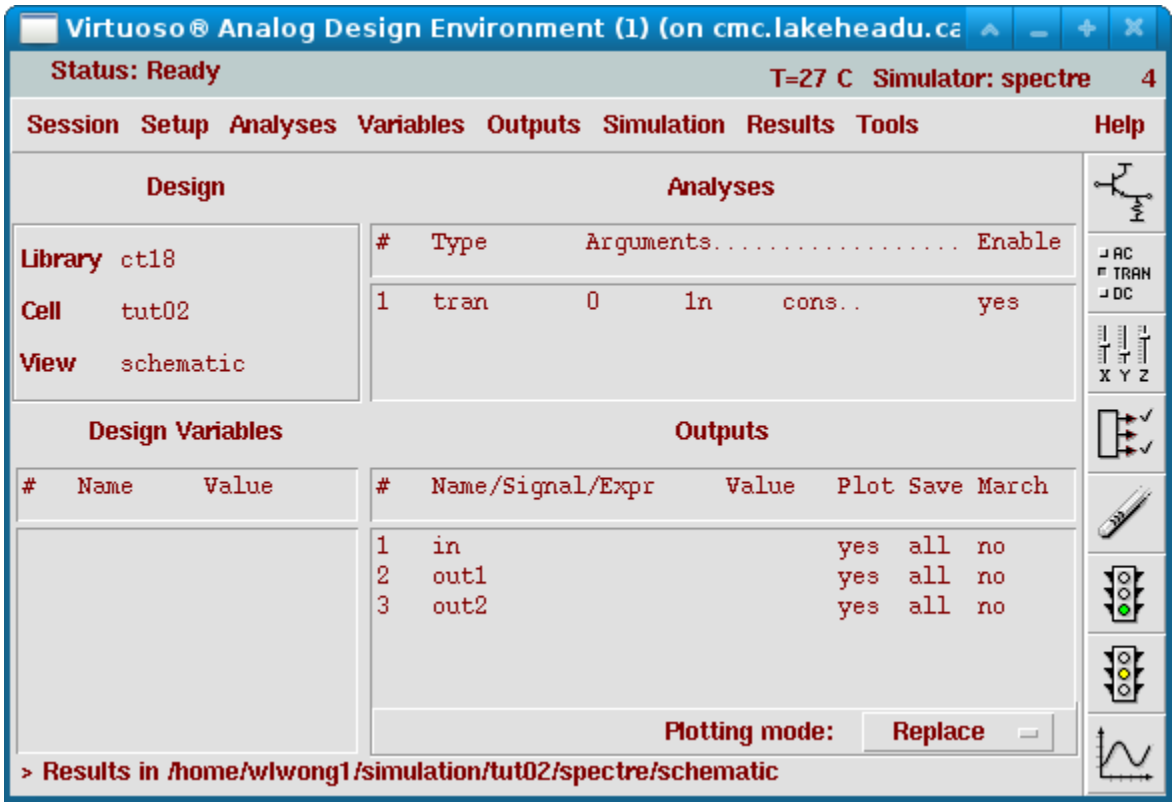




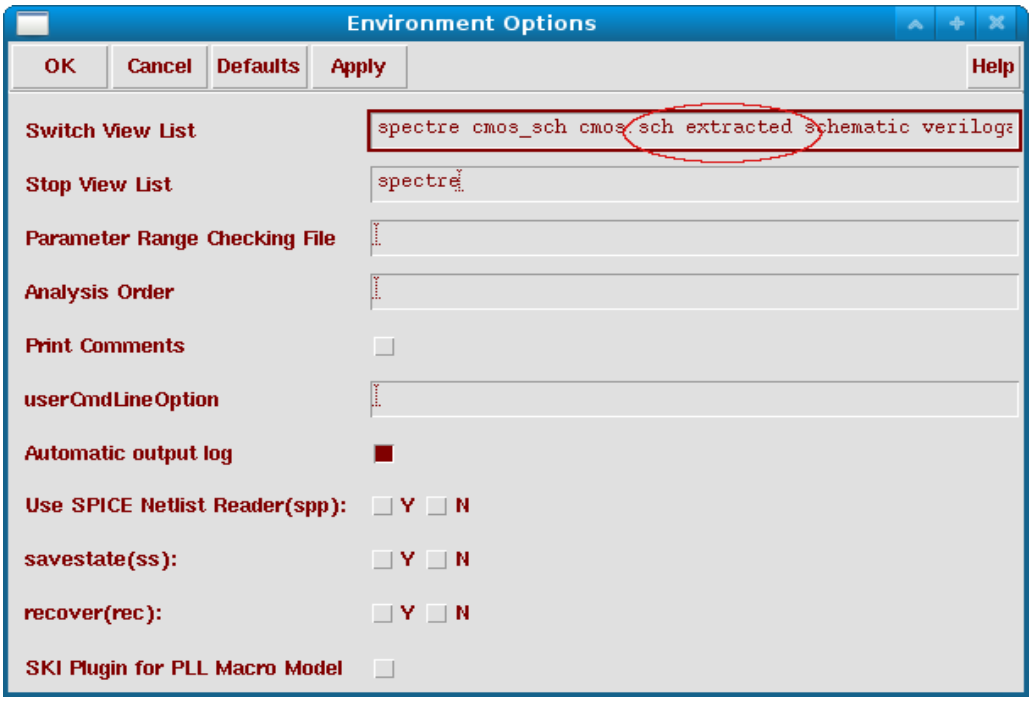
Next, create a new schematic in the same library that you are using to test the new symbol. The new created symbol can be instantiated as usual like other components, except that it located in is the Cell you are working with.



Load the Analog Design Environment and set up a transient analysis as shown below.



In the ADE menu bar, click **Setup** → **Environment**. Add the word '`extracted`' to the **Switch View List** line. Click **OK** and run the netlist.



The simulation results are below.