ENGI 5131 --- Tutorial 3

Layout Creation

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Winter 2013 – Revised 2017

Objective:

Create a CMOS inverter layout with Cadence Virtuoso.

Please refer to the TSMC 0.18 μm Design Rules Manual for abbreviations and terminologies. The file is located in /CMC/kits/cmosp18/Doc/CMOSP18designRulesLogic.pdf

1. Schematic Diagram

Create a schematic diagram (Figure 1) as depicted below.

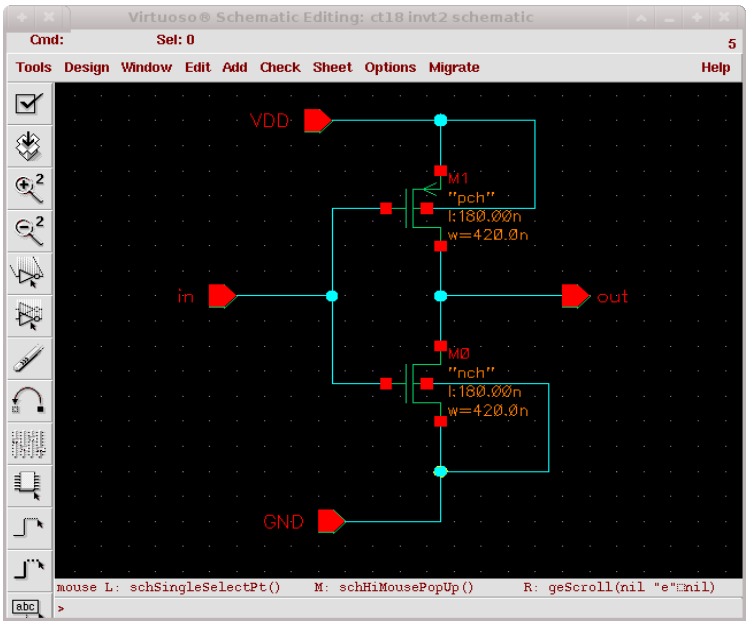


Fig. 1: Schematic diagram. Change transistor width and length to 420 nm and 180 nm.

2. Create Layout Cellview

After finishing the schematic diagram, check and save it.

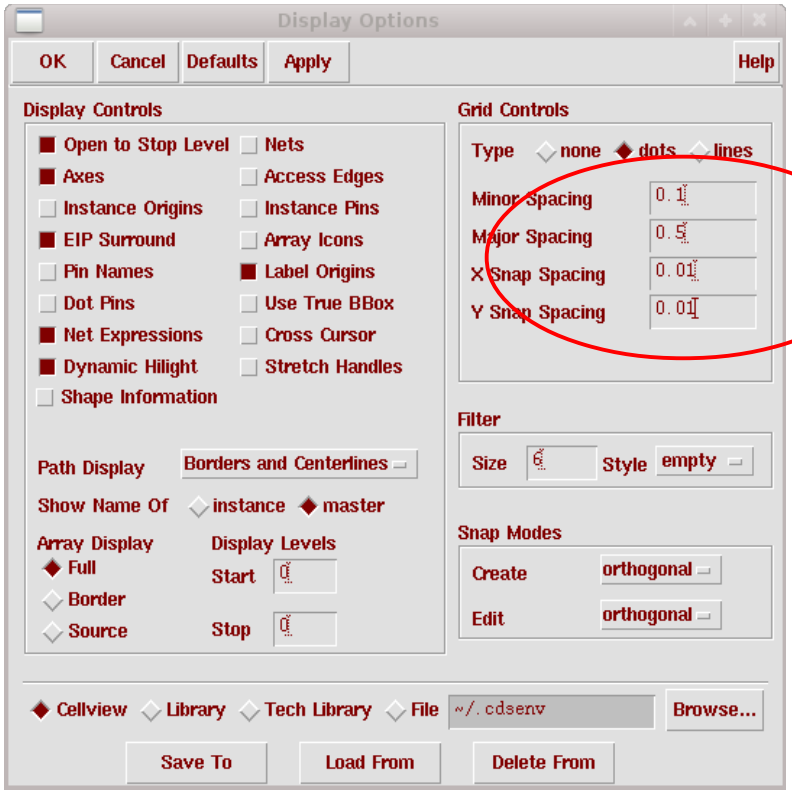
1. In the Schematic Editor, select **Tools-> Design Synthesis -> Layout XL.**

2. A small window will pop up. Choose **Create New.**

3. Confirm that the content in the **View Name text box** is "**layout**", and the design tool is "**Virtuoso**". Click **OK** to continue. The Virtuoso XL layout Editor and LSW (Layer Selection Windows) will display.

4. In the Layout Editor menu bar , select **Option** -> **Display**. Change the settings of the display space as follows:

Minor Spacing	0.1
Major Spacing	0.5
X Snap Spacing	0.01
Y Snap Spacing	0.01



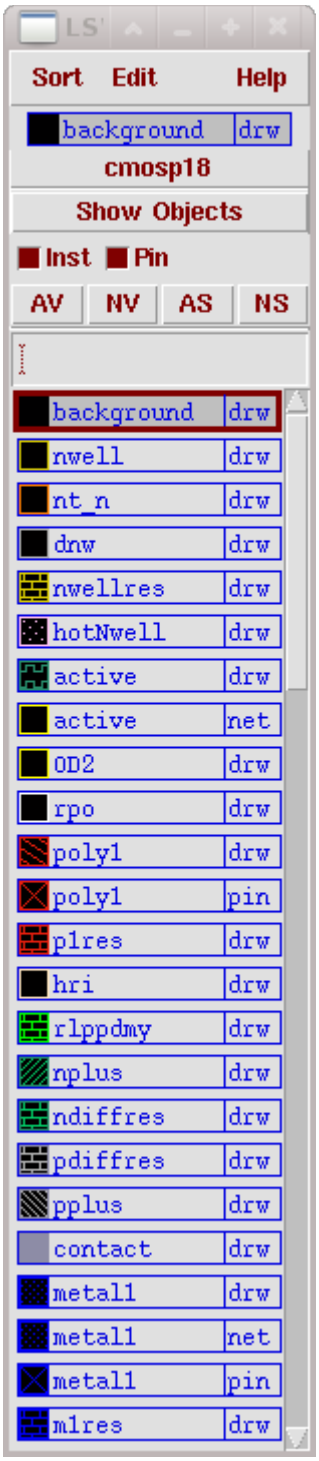


Fig. 2: Layer Selection Windows (LSW)

Here are some useful hot keys.

Drawing functions:

r	draw rectangle
p	draw path

Editor functions:

c	Copy
f	Zoom fit
i	Instance
k	Ruler
K	Erase all rulers
m	Move
ctrl r	Redraw
s	Stretch the edge of an object
q	Properties

3. Create PMOS layout

Let's create a PMOS transistor with **W=0.42 µm** and **L=0.18 µm**. We will need to draw the gate, active region, p+ diffusion region, contacts, substrate, and n-well.

1. To create a ruler, click the ruler icon on the left hand side of the Layout Editor.

2. Choose the **"poly1 dwg"** layer from the LSW, Figure 2. Select **Create-> Rectangle** or use the hot key 'r' to create a rectangle with a length of 0.18 µm and a width of more than 1.50 µm.

3. Select the **"active dwg"** layer; draw a rectangle with X = 1.14 µm and Y = 0.42 µm as shown in Figure 3.

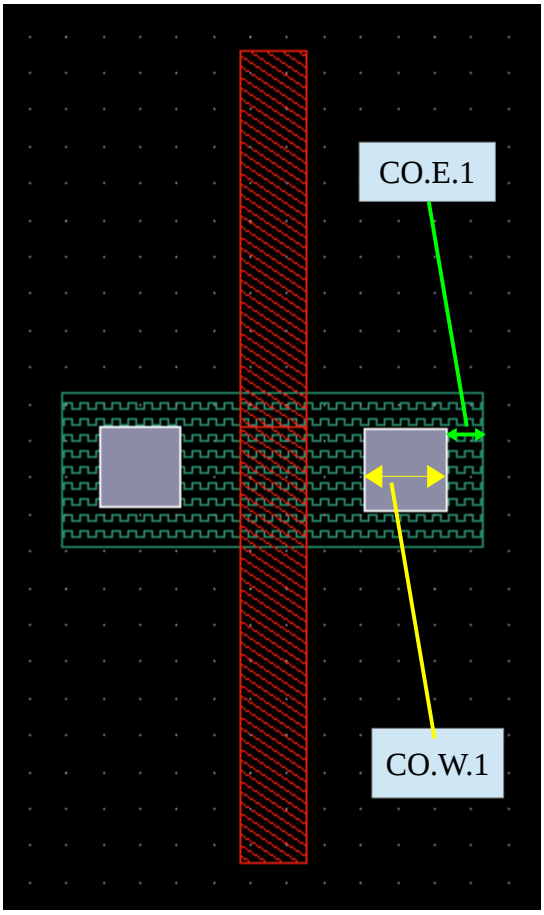


Fig. 3: Create the poly1, active, and contact layers.

Yellow arrows: CO.W.1, Green arrows:CO.E.1
Red rectangle is poly 1, dark green block defines active region, and grey squares are Contacts

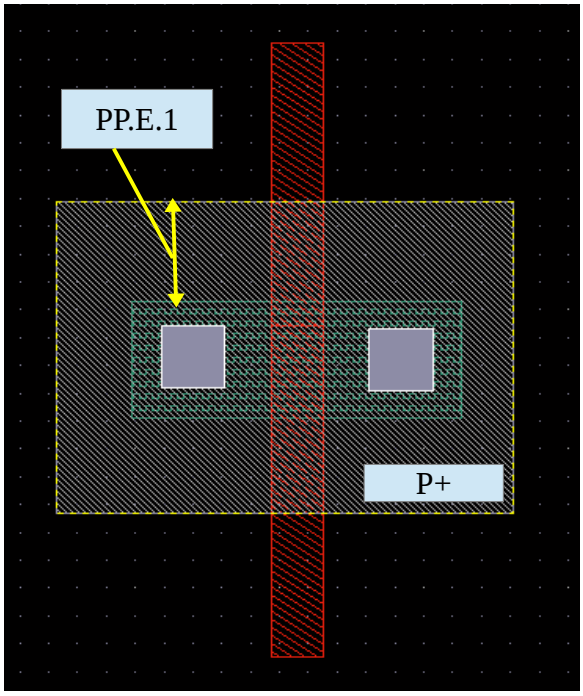


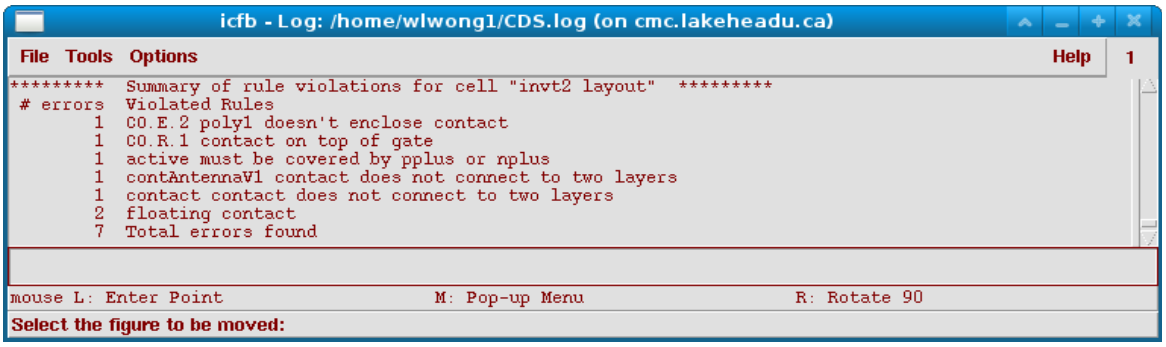
Fig. 4: Draw "P plus" layer.

Yellow arrows is PP.E.2. Yellow arrows: PP.E.2
Grey area defines P-plus

4. On page 42 of the Design Rule manual, find the maximum and minimum width rule (**CO.W.1)** for contacts. Select the **"contact dwg"** layer form LSW and create a square contact.

5. On page 28, find the minimum clearance between active (OD) and contact (CO) **(CO.E.1)**, place the contacts as shown in the Figure 3.

6. Run the DRC. In the Layout Editor's menu, click **Verify-> DRC -> OK.** All design rule violations will be listed in the Command Interpreter Window (CIW). For now, ignore any violations except rule **CO.W.1** and **CO.E.1**. Correct **CO.W.1** and **CO.E.1** errors by stretching or relocating the contacts. Below is an example.



7. To clear all markers, select **Verify-> Marker-> Delete All** from the Layout Editor menu.
8. Press **ctrl-r** to redraw the screen and hit 'f' to zoom to fit.

Optional: Click **OK** and select **Option->Layout Editor.** Select **"Gravity on"** and change the **Aperture** to **0.01**. Click **OK**, zoom fit and move your mouse around the layout. Observe the behaviour of the pointer when it moves close to any objects. The **Aperture** environment variable specifies how close it has to be in order to snap to an object. Hot key 'g' toggles gravity function on and off.

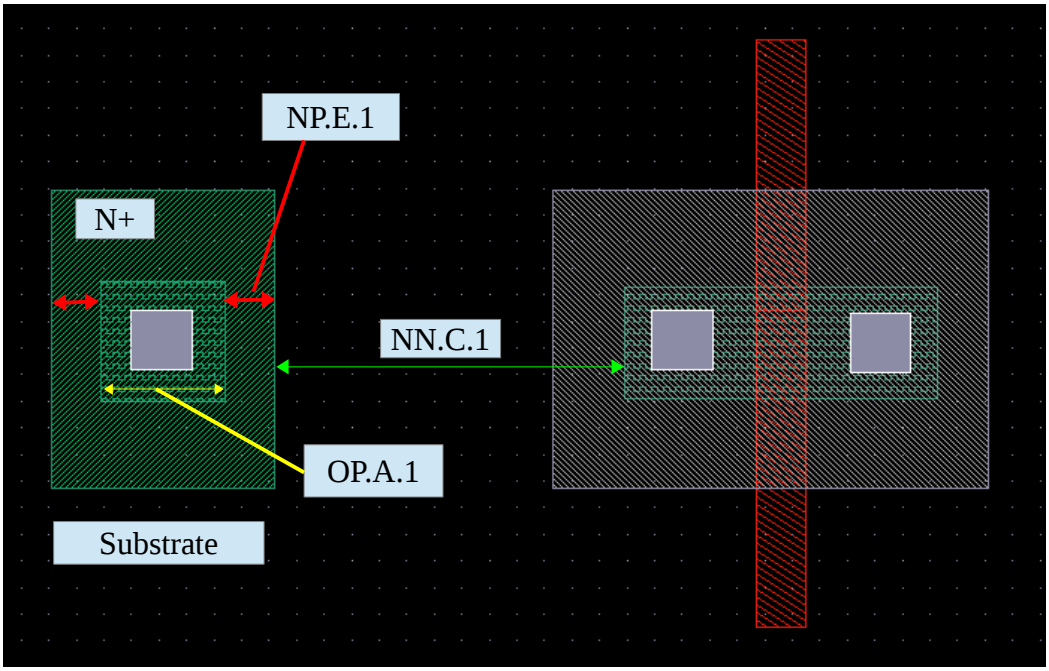


Fig. 5: Creating PMOS substrate.

Red: NP.E.1 , Yellow: OP.A.1, Green: NP.C.1. The large green area is n+ diffusion for the substrate. The green square in the middle is active or N+OD.

9. On page 38, find **PP.E.2 ,** the minimum extension of **pplus (p+)** and (**P+OD**) p+ active region. It is the vertical blue double arrow in the figure.

10. Select the **"pplus dwg"** layer and draw a rectangle as illustrated in Figure 3. Run DRC and confirm that **PP.E.2** is not violated.

Next, we will create a substrate contact on the left side of the transistor.

11. Select the **"contact dwg"** layer; draw a square contact (**CO.E.1**) as depicted in Figure 5.

12. On page 23 , find **OD.A.1,** the minimum area of N+ active. To define the active region for the substrate, select the **"active dwg"** layer and create the smallest square with an area given by **OD.A.1**. Align the substrate contact and active region as depicted in Fig 4.

13. Find the minimum overlap from N+ to its active (OD) region (**NP.E.1**) on page 33.

14. Select the "**nplus dwg"** layer; draw a rectangle of the same height as P+ region and wide enough to cover the active region (**NP.E.1**).

15. Find the minimum clearance from p plus active region (grey) to n plus region (green) (**NP.C.1**) on page 33. See the green arrows in Figure 5.

16. Place the substrate as close to the PMOS as possible. See Figure 6.
17. Run DRC and confirm no **NP.C.1** and **NP.E.1** violations.

18. Select the **"nwell dwg"** layer and create an N-well around the transistor as shown in Figure 6.

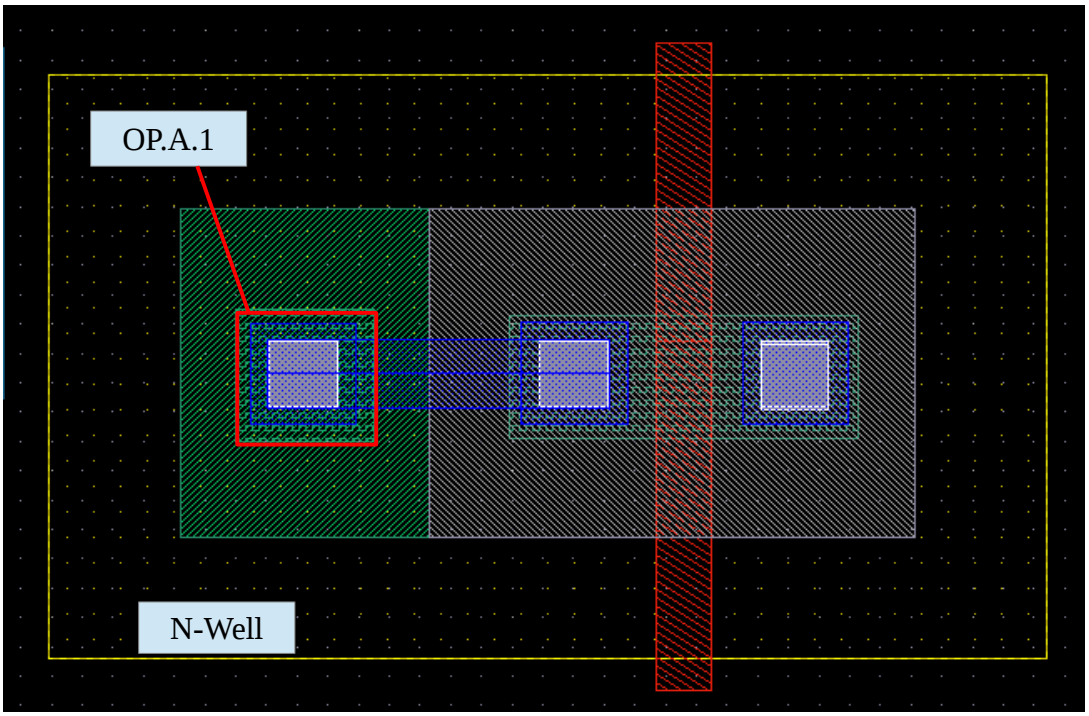


Fig. 6: PMOS transistor. The yellow box defines N-Well for PMOS transistor. Minimum size of N+ active are limited by the rule OD.A.1.

19. Before we start to make any metals, let's turn off all other layers except poly 1, contact and metal 1 layers. In the LSW window, select the contact layer; click the **NV** button; select the **"metal 1 dwg"** layer and the **"poly 1 dwg"** layer. Return to the Layout Editor and press **ctrl-r** to redraw the display.

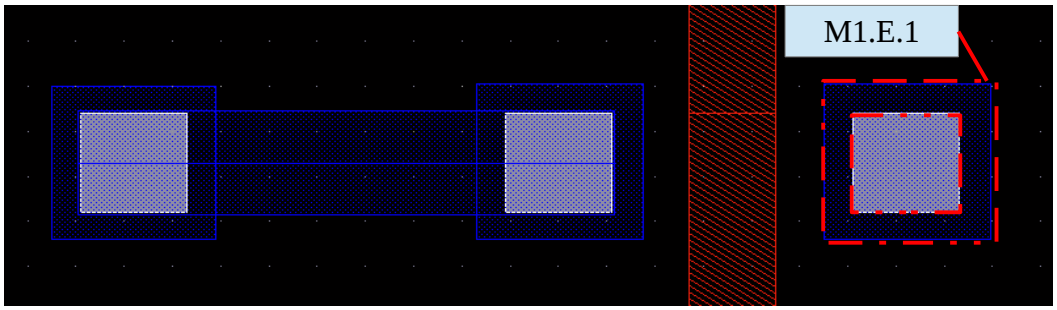


Fig. 7: Metal contacts. Blue colour rectangle represents metal 1.

Yellow: M1.E.1

20. Find the minimum extension of metal 1 and contact (**M1.E.1**) on page 44.

21. Select the **"Metal 1 dwg"** layer; create a smallest possible metal 1 square and place it on top of contact as shown on Figure 7. Then, make a connection between metal contacts with the path function (hot key 'p') or rectangle function (hot key 'r').

22. To makes all layers visible again, click the **AV** button in the LSW; redraw (**ctrl-r**) the display and zoom fit ('f').

23. Verify the layout; click **Verify-> DRC -> OK.** Confirm there is no **M1.E.1** violation.

24. To investigate any specific error, click **Verify -> Markers -> explain.** Then, click on any blinking objects in the Layout Editor. For now, ignore any errors about floating poly, minimum metal area and power/ground label, but correct any other errors as need.

25. To clear markers, select **Verify-> Marker-> Delete All** from the Layout Editor menu.

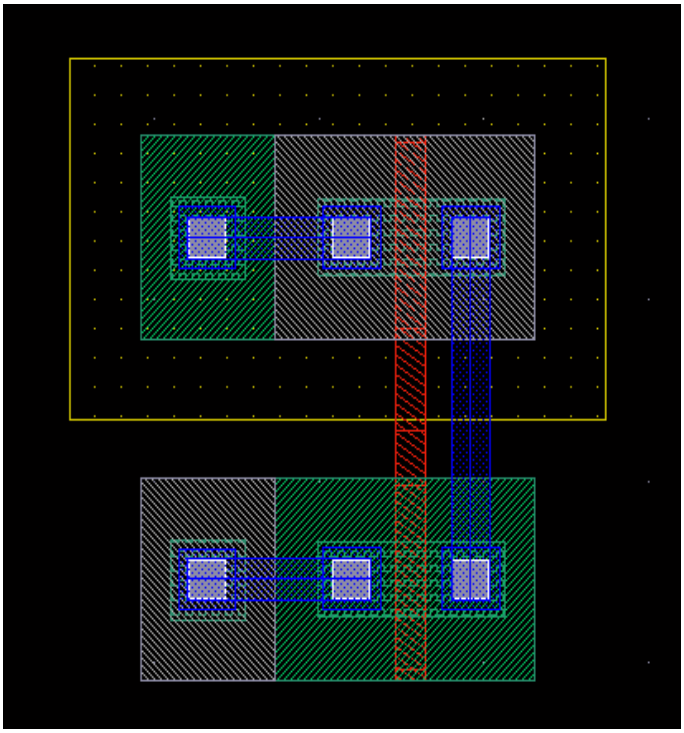


Fig. 8: Copy the PMOS layout and paste it in the area below. Change the PMOS diffusion layer accordingly.

4. Create NMOS Layout

1. Copy ('c') the entire PMOS transistor to the area below the PMOS transistor as shown on Figure 8.

2. Highlight the P+ region (**pplus**) of the new transistor and change it to N+ (**nplus**) using the properties function. Similarly, change the substrate area from **nplus** to **pplus**. Now, a new NMOS transistor with the same dimension of the PMOS transistor is created.

5. Inverter

1. Connect the gates with polysilicon 1 as shown in Figure 9.

2. Insert the metal contact and metal 1.

3. Join the drain terminals with metal 1.

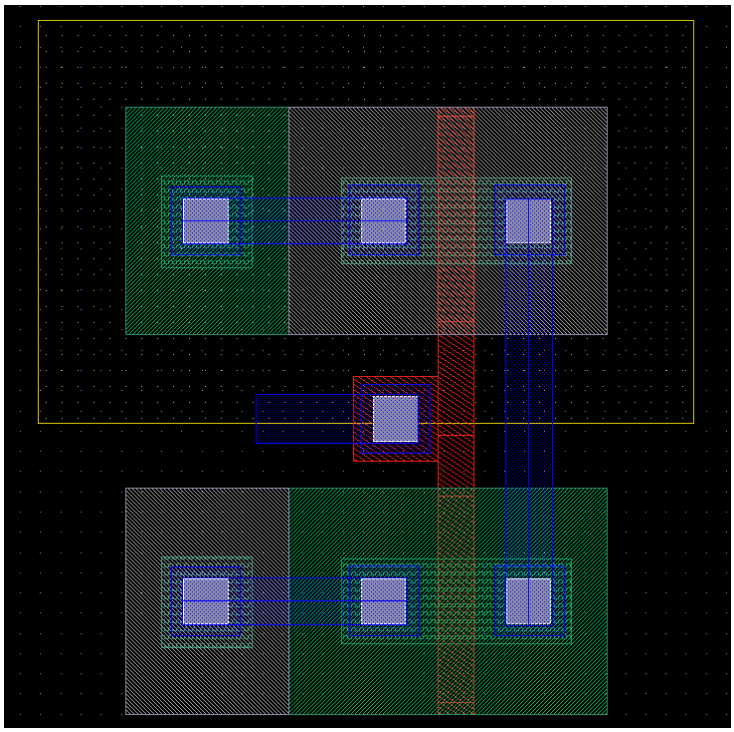


Fig. 9: Inverter Layout. Create the NMOS transistor by copying the PMOS to the space below.

6. Create Shape Pins

1. In the Layout Editor, click **Create-> pin.** Change the dialog to **Create Shape Pin**.

2. In the Terminal Names box, enter '**out**'. Click the **Display Pin Name Option**, change the Height to **0.15**, confirm that "**text dg**" has been selected for layer. Click ok to continue.

3. Change I/O type to **"output"**.

4. Go to LSW and select the **"metal1 pin"** layer. (not "metal1 dwg")

5. Draw a rectangular pin on Metal 1.

6. Repeat step 2 to 5 for terminal **vdd!, gnd!** and **in.**

7. Figure 10 shows the final layout. Verify your layout with DRC.

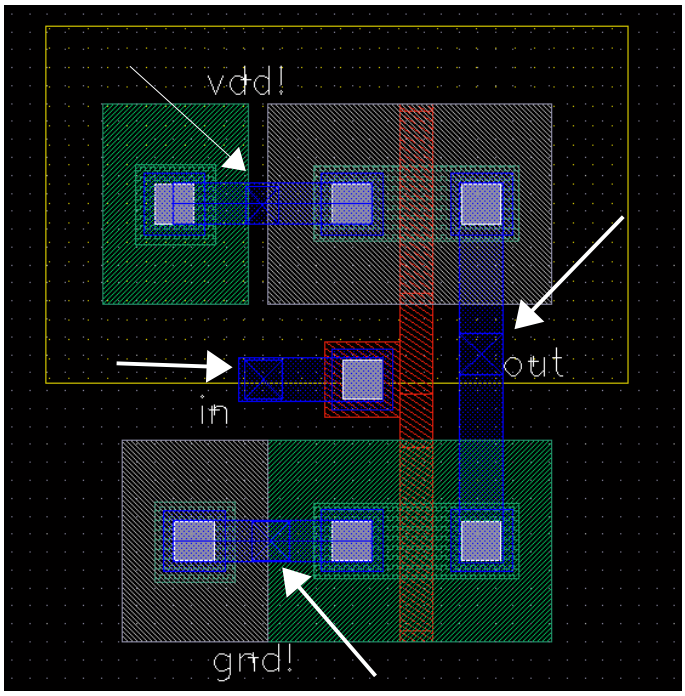


Fig. 10: Inverter Layout with Pins