ENGI 5131 --- Tutorial 1

Using the Schematic Editor and Analog Environment

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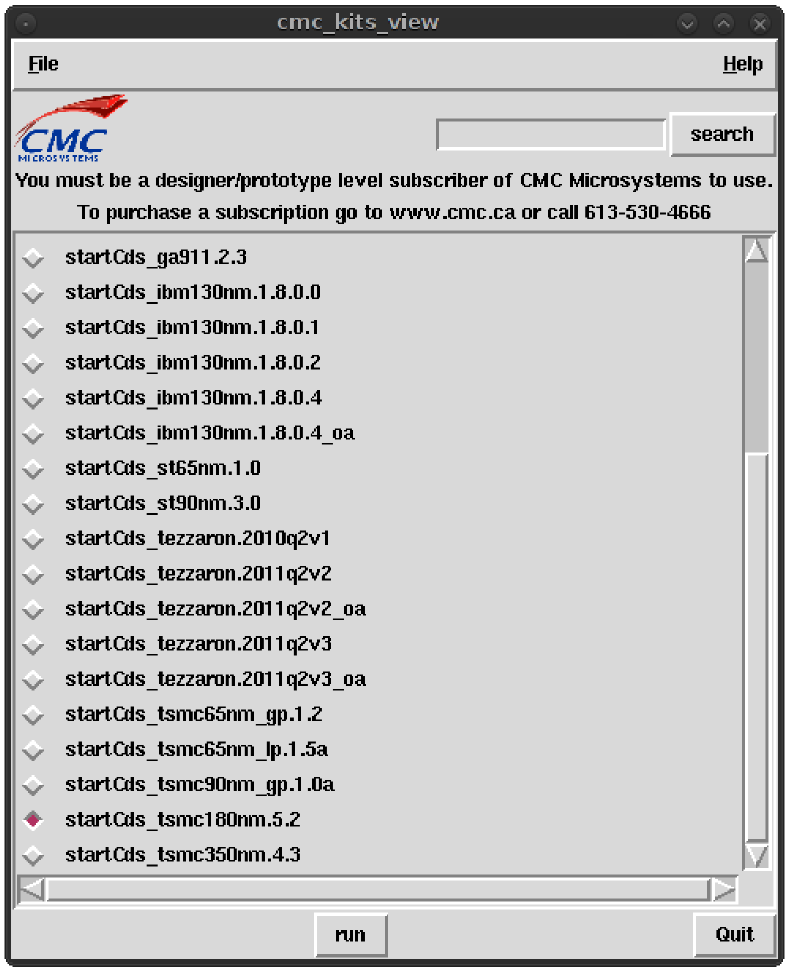
1. Starting Cadence

To start Cadence, open a terminal and type

```
mkdir design
cd design
/CMC/bin/goCadence
```

The following dialog box should appear:



After selecting “run”, you should now see the ICFB log and a “What's New” window appear. Close “What's New”.

[Tip] If anything goes terribly wrong in Cadence during any part of design or simulation, the ICFB log will be a good place to check. Closing the ICFB log quits Cadence.

2. Creating the Library and Cell

At the top of the ICFB log window, select Tools → Library Manager. At the top of the Library Manager window, select File → New → Library. In the Name field, enter “tutorial1”, and select OK.

A new window will appear called “Technology File for New Library”. We want to implement the new project in the .18µm (or “point eighteen”) CMOS technology, so select “Attach to an existing techfile”, and select OK. Another new window will appear called “Attach Design Library to Technology File”. Beside “Technology Library” there is a dropdown box whose default selection is “CMCpcells”. Change that to “cmosp18” and select OK.

You should see the Library Manager again. Under the Library heading, you should be able to scroll down and see “tutorial1”, your new library. Select it. At the top of the Library Manager window, select File → New → Cell View. The library name should show “tutorial1”. For the Cell Name field, type “csamp”. The view name should show “schematic” and the tool should show “Composer-Schematic”, the visual circuit editor for the Cadence tool suite. The Virtuoso Schematic Editor should appear, and the Library Manager should show “csamp” under the Cell heading. You can close the Library Manager.

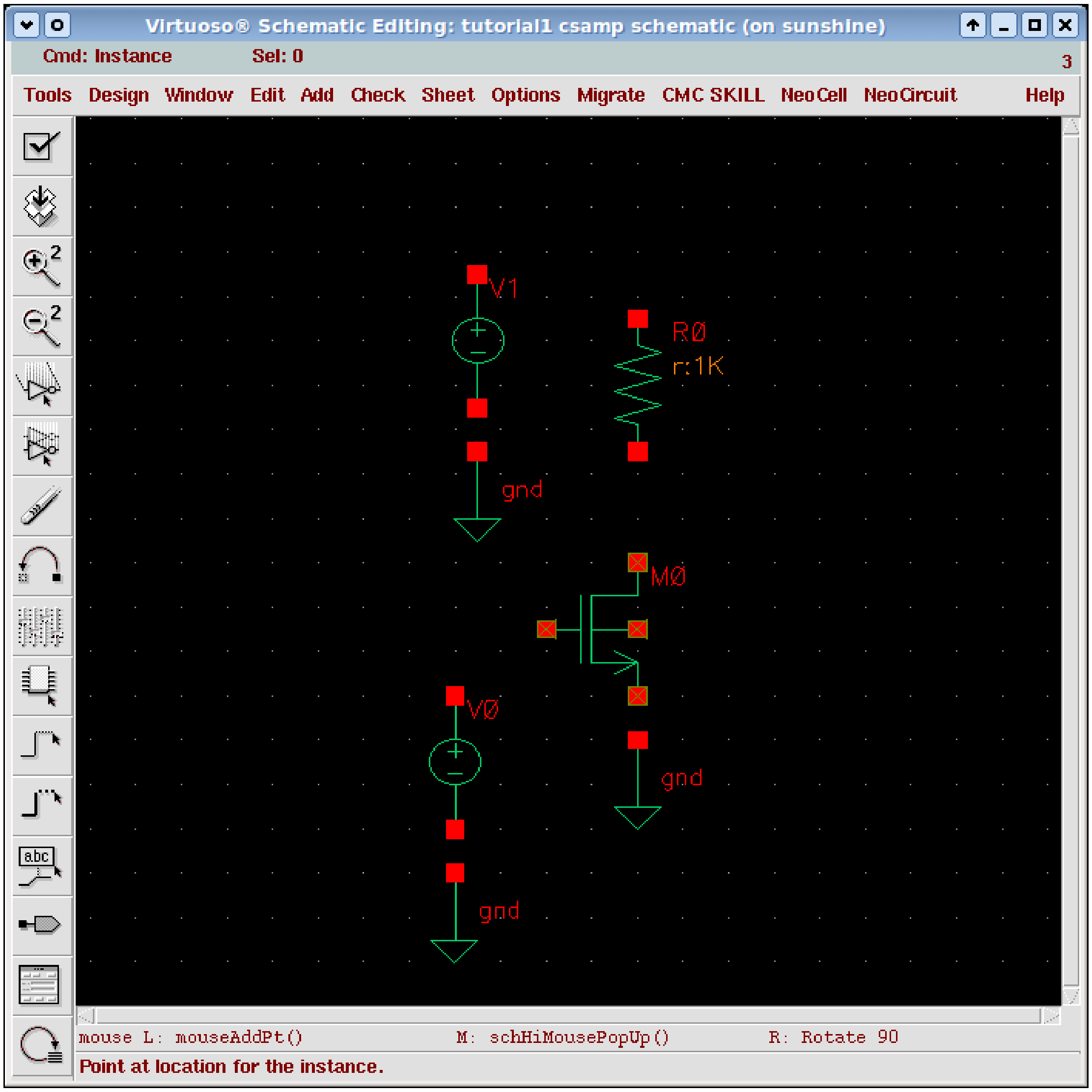


Figure 1: The circuit, with all component instances placed but no connections.

3. Entering the Circuit

To create the common-source amplifier, the transistors, voltage supply, resistor and grounds must first be added. On the toolbar to the left of the Virtuoso Schematic Editor, select the button with the icon of an eight-pin chip with the tool tip “Instance”, or simply press the “i” key. If you want to get an idea of the different components available you can select Browse, but if you already know exactly what you need you can type in the Library, Cell and View fields.

In the new Add Instance window, enter “analogLib” for the Library, “nmos4” for the Cell, and “symbol” for the View. The other fields do not need to be modified. Select “Hide” to get back to the schematic. Your cursor icon is now the symbol of a transistor. Every time you left-click, it will place an NMOS transistor. It will keep doing this until you press the escape key. We only want one transistor, so click once in the middle of the schematic and then press escape.

Using the same steps, add two analogLib/vdc/symbol, one analogLib/res/symbol, and three analogLib/gnd/symbol so that your circuit looks like Figure 1.

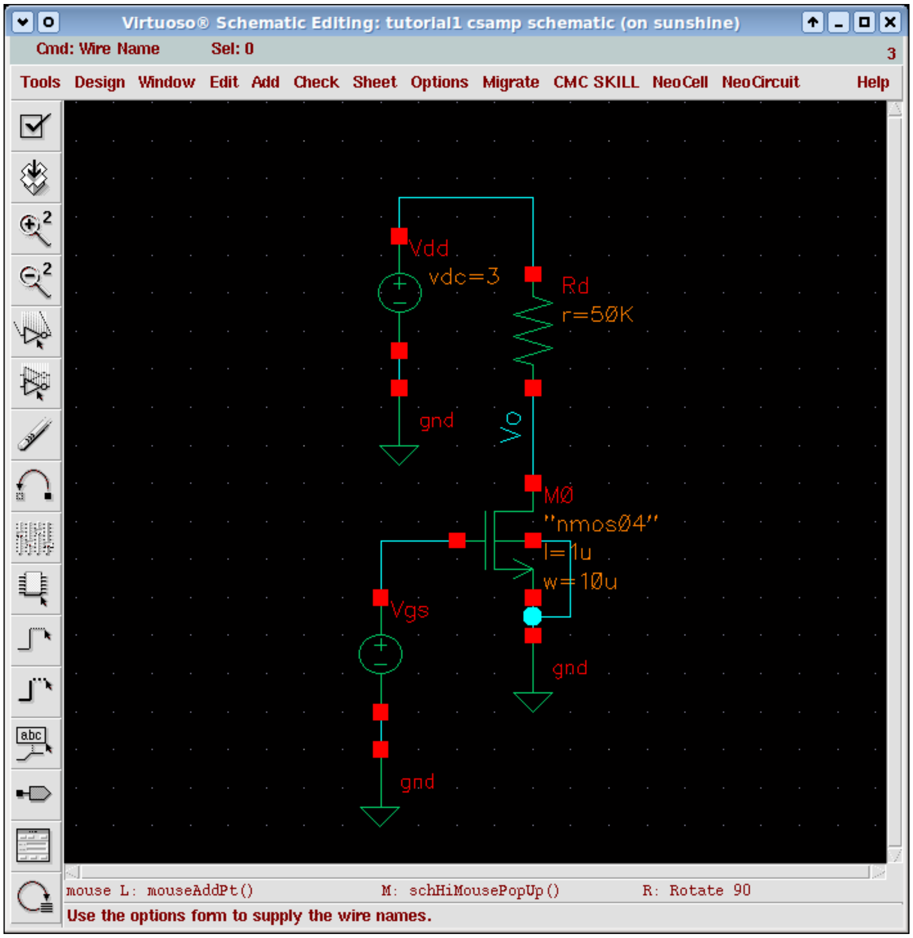


Figure 2: The finished circuit, with properties, nets and net names.

To create the connections (a.k.a. nets a.k.a. wires) between components, move the mouse cursor over a red terminal. Tap the W key, then left click where you want the wire to end. Once you are done, click on the check mark on the left toolbar with the tool tip “check and save”. If you have missed any nets, there will be flashing yellow terminals.

To set the properties of a component, drag a box over it to select it. Then select the ninth button on the left toolbar that looks like an audio mixer (Property), or press Q. Set the following properties:

Supply voltage

- Instance Name: Vdd
- DC voltage: 3

Gate-source voltage

- Instance Name: Vgs

Drain resistor

- Instance Name: Rd
- Resistance: 50k

Transistor

- Model name: nmos04
- Width: 10u
- Length: 1u

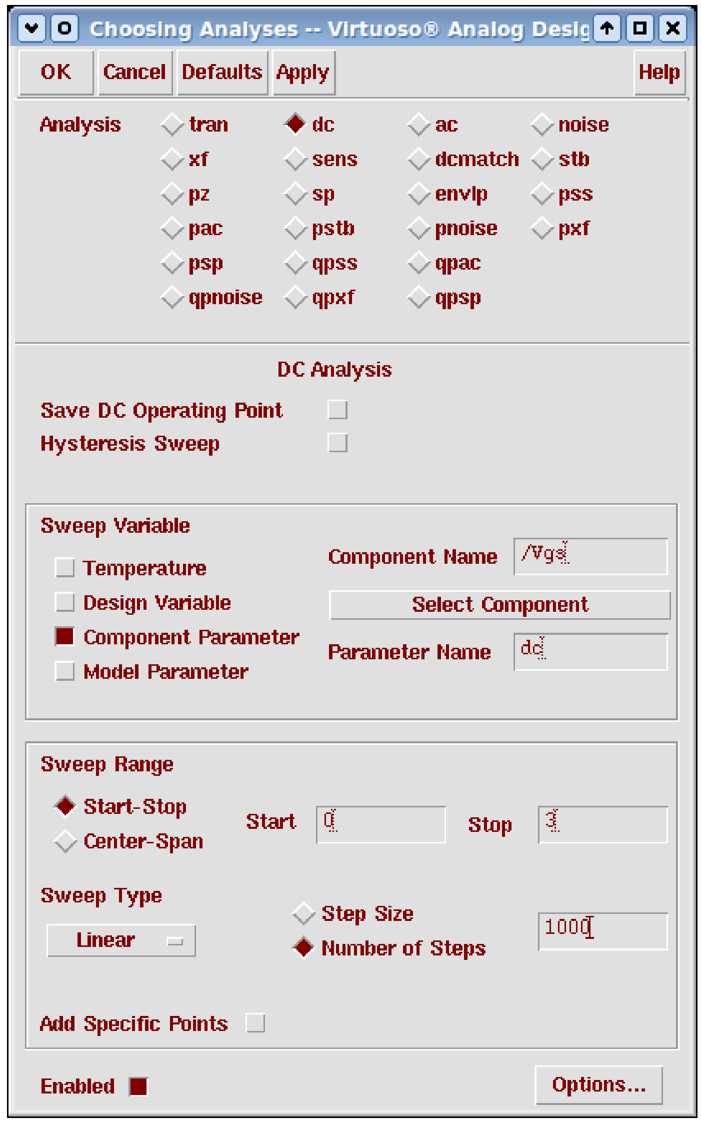


Figure 3: The simulation setup.

Naming nets is very important to keep track of signals in complicated circuits. To name the output net, click on the “abc” button on the left toolbar (Wire Name). In the Names field, type “Vo”, then press enter. Left-click on the net above the drain of the transistor.

Once all of the above steps are done, press “check and save” again. The ICFB log should show “Schematic check completed with no errors”. The finished circuit is shown in Figure 2. During the next simulation steps, keep the schematic editor window open.

4. Setting up the Simulation

At the top of the schematic editor window, select Tools → Analog Environment. The Virtuoso Analog Design Environment window (the Cadence circuit simulator) will appear. Select Setup → Model Libraries. In the Model Library Setup window, in the Model Library File field, enter

```
/CMC/kits/models/textbook_mos.mod
```

This model controls the behaviour of transistors in simulation. Once the file name is typed in, select Add, then OK.

To set up the independent variable in the simulation (time, or a certain voltage, or a certain device parameter for instance) you need to go to the Choosing Analyses window. This can be reached with Analysis → Choose, or the AC/TRAN/DC button on the toolbar. Choose DC analysis. Under the Sweep Variable options, select Component Parameter.

Click on Select Component. Switch to the schematic editor window. Move the cursor over Vgs. When a dotted yellow border appears, left-click. Select “dc” and then OK. Back in the Choosing Analyses window, “/Vgs” should appear for the Component Name, and “dc” should appear for the Parameter Name. (If you know exactly what you're doing, you could just type these in.)

Still in the Choosing Analyses window, in the Sweep Range options, make sure “Start-Stop” is selected, and then enter 0 for Start and 3 for Stop.

The simulator will be considering the circuit's behaviour for values of Vgs between 0V-3V. The Sweep Type determines how many values there are and how they are spaced. For many purposes, “automatic” is fine, but we want higher resolution (at the cost of slower simulation). Select a linear sweep type with 1000 steps.

The Choosing Analyses window should look like Figure 3. Select OK.

5. Running the Simulation

We need to specify which circuit variables should be monitored. At the top of the Virtuoso Analog Design Environment window, select Outputs → To Be Plotted → Select On Schematic. Switch to the schematic editor, and click on the Vo net. It will change colours and become a dashed line instead of a solid one. Back in the analog window under Outputs, you should see Vo.

To simulate, press the green light icon (Netlist and Run) or select Simulation → Netlist and Run. You should get an output similar to that of Figure 4.

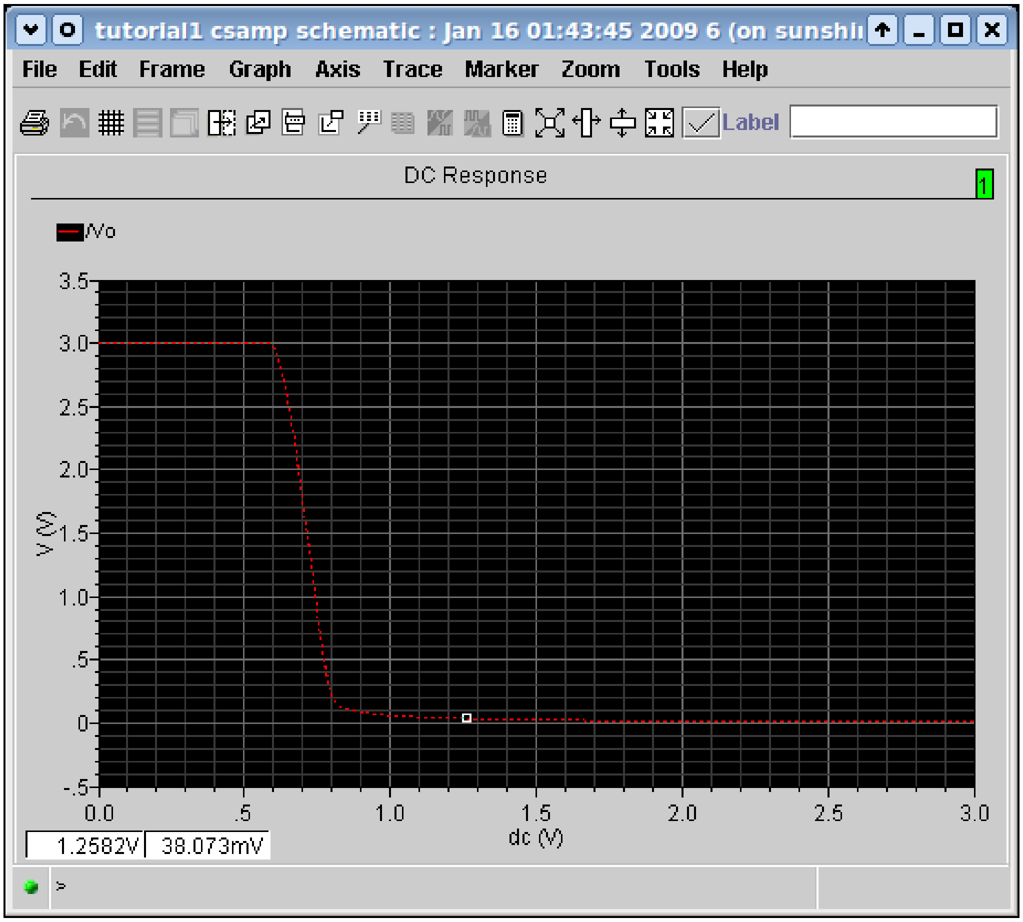


Figure 4: Simulation output.

By moving around the cursor, you can see x and y values on the lower left. Using two points in the transition region of the output, manually calculate the maximum small-signal gain:

$$A_V = \frac{V_{O2} - V_{O1}}{V_{GS2} - V_{GS1}}$$

It should be somewhere around -17.8.

6. (Optional) Automatic Gain Determination

It would be good to verify the accuracy of your calculation, and to get some practise with WaveScan functions. WaveScan is the Cadence tool to take care of plotting and mathematical analysis of simulation results.

Return to the analog window. In the Choosing Analyses window, change the range from 0V-3V to 0.5V-1V. (This increases the resolution of the simulation over the transition region of the output.) Click on the toolbar button with the check marks (Setup Outputs). In the Name field, enter Max Av. In the Expression field, enter

```
ymin(deriv(VS(“/Vo”)))
```

This takes the minimum value of the instantaneous derivative of the output voltage with respect to the input voltage. Select Add, then OK. Press “Netlist and Run” again. In the Outputs section of the analog window, beside Max Av, -17.83 appears.

There are many very useful WaveScan functions available to help analyses; a full guide PDF can be found on the course website.

7. Save and Close

At the top of the analog window, select Session → Save State. Enter “tutorial1” in the Save As field and select OK. Close all Cadence windows. When the Save Display Information prompt appears, hit Cancel.

Debugging Note

It is important to close Cadence when you are done with it. If there has been a crash and the software aborted abnormally there are two important things you must do.

1. Look for and delete any files called “core” in your circuit directories. These are memory dumps that are created after crashes and take up a **huge** amount of space on the disk. Eventually they will exhaust your space quota and nothing will work.
2. Look for and delete any files with the extension “.cdslck”. These are lock files that Cadence creates when the program is running. If the program dies abnormally, this lock file will not be deleted, and you will not be able to save any changes to your design the next time the program is run unless you delete it yourself.